Energy Transparency from Hardware to Software

Why SW engineers are key to energy efficient computing

Kerstin Eder

Design Automation and Verification, Microelectronics Verification and Validation for Safety in Robots, Bristol Robotics Laboratory









19 March 2012 Last updated at 17:34



Free mobile apps 'drain battery faster'

Free mobile apps which use third-party services to display advertising consume considerably more battery life, a new study suggests.

Researchers used a special tool to monitor energy use by several apps on Android and Windows Mobile handsets.

Findings suggested that in one case 75% of an app's energy consumption was spent on powering advertisements.



Like many games, Angry Birds has a free version supported by targeted advertising

Report author Abhinav Pathak said app makers must take energy optimisation more seriously.

Energy Aware System Design

Hardware Design

- Power management largely in domain of Hardware Design
 - Considerations to minimize/optimize
 - Dynamic (switching) and static (leakage) power
 - On-chip power management

- Modes: on, standby, suspend, sleep, off

Development of low power electronics

Where can the greatest savings be made?

Greater Savings at Higher Levels

Why Optimize Power at the Architecture?



Power Optimization Potential

news

ElectronicsWeekly 15-21 June 2011 | No. 2472

LOW POWER

Lack of software support marks the low power scorecard at DAC

ne of the panels at the Design Automation Conference (DAC), which took place in California in early June, set out to get an idea of how well the industry is doing at delivering lower-power systems.

It is becoming clear, *writes Chris Edwards*, that the system level is currently the missing link.

Processes can deliver some gains – and Globalfoundries' Andrew Brotman was able to outline some of the features that the foundry has put into its recently launched low-power high-k, metal gate (HKMG) process.

FinFETs should bring power down as those processes become available, although they are not the only eptions. But if the software keeps cores active for no good reason, the lower switching power per bit processed won't deliver a realised saving.

In his keynote speech Gadi Singer, vice-president IAG and general man ager of the SoC enabling group at Intel Corporation, said that with limited software support, dedicated low-



Intel waits for better low-power software control

power circuitry could save maybe 20% in a typical multimediaoriented core.

Make the software controlling it

better at controlling the power states and that difference could be three to five times.

During an afternoon panel discus-

sion Ambrose Low, director of design engineering at Broadcom said: "We have hundreds of knobs in the hardware to turn power down.

"The question is whether we can take the actual use-cases into consideration and optimise the software to power the logic circuits down. We still have a long way to go."

Ruggero Castagnetti of LSI argued that the desire to do more in software will grow.

"As we see power limits and targets becoming unachievable, customers will be willing to go to that extra step. There is a challenge that needs to be addressed and we have to do more on the systems side," Castagnetti said.

"We should put a challenge to the software designers to see how much power they can save," he added.

Chris Edwards writes the Low-Power Design Blog (enabled by Mentor Graphics) on ElectronicsWeekly.com

www.electronicsweekly.com/ew-blogs/

Wasted Potential



Huge advances have been made in powerefficient hardware.

BUT – potential energy savings are wasted by

- software that does not exploit energy-saving features of hardware;
- poor dynamic management of tasks and resources.



- Software controls the behaviour of the hardware
 - Algorithms and Data Flow
 - Compiler (optimizations)
 - Traditional SW design goals: performance, performance,
 performance,





- Software engineers often "blissfully unaware"
 - Implications of algorithm/code/data on power/energy?
 - Power/Energy considerations
 - at best, secondary design goals
- BUT the biggest savings can be gained from optimizations at the higher levels of abstraction in the system stack
 - Algorithms,
 - Data and
 - -SW



6.3. SOFTWARE DESIGN FOR LOW POWER

KAUSHIK ROY AND MARK C. JOHNSON School of Electrical and Computer Engineering Purdue University West Lafayette, Indiana, U.S.A.

1. Introduction

It is tempting to suppose that only hardware dissipates power, not software. However, that would be analogous to postulating that only automobiles burn gasoline, not people. In microprocessor, micro-controller, and digital signal processor based systems, it is software that directs much of the activity of the hardware. Consequently, the software can have a substantial impact on the power dissipation of a system. Until recently, there were no efficient and accurate methods to estimate the overall effect of a software design on power dissipation. Without a power estimator there was no way to reliably optimize software to minimize power. Since 1993, a few researchers have begun to crack this problem. In this chapter, you will learn

Aligning SW Design Decisions with Energy Efficiency as Design Goal

Key steps*:

- "Choose the best algorithm for the problem at hand and make sure it fits well with the computational hardware. Failure to do this can lead to costs far exceeding the benefit of more localized power optimizations.
- Minimize memory size and expensive memory accesses through algorithm transformations, efficient mapping of data into memory, and optimal use of memory bandwidth, registers and cache.
- Optimize the performance of the application, making maximum use of available parallelism.
- Take advantage of hardware support for power management.
- Finally, select instructions, sequence them, and order operations in a way that **minimizes switching** in the CPU and datapath."

^{*} Kaushik Roy and Mark C. Johnson. 1997. "Software design for low power". In Low power design in deep submicron electronics, Wolfgang Nebel and Jean Mermet (Eds.). Kluwer Nato Advanced Science Institutes Series, Vol. 337. Kluwer Academic Publishers, Norwell, MA, USA, pp 433-460.

Information on energy usage is available for programs:

- ideally without executing them, and
- at all levels from machine code to high-level application code.

Transparency



Transparency



Transparency



* Dati da elaborazione ENEA (riterimento anno 2008)

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Why Energy Transparency?



Energy transparency enables a deeper understanding of how algorithms and coding impact on the energy consumption of a computation when executed on hardware.

Measuring the Energy Consumption of Computation



The Showstopper 🛞



Measuring Power

Measure voltage drop across the resistor

I = Vshunt / Rshunt to find the current

Measure voltage at one side of the resistor

 $P = I \times V$ to calculate the power



The Power Monitor





Measuring Power

Repeat frequently, timestamp each sample Measure voltage drop across the resistor

Measure voltage at one side of the resistor

I = Vshunt / Rshunt to find the current

 $P = I \times V$ to calculate the power



Measuring Energy



Time

How much data?

Currently 500,000 Samples/second 6,000,000 S/s possible in bursts

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Open Energy Measurement Board



Energy Measurement



Online Demo

Dynamic Energy Monitoring

The EACOF

Symposium on Applied Computing

A simple Energy-Aware COmputing Framework https://github.com/eacof

High Level











Comparing Sorting Algorithms

Sorting of integers in [0,255]

		Data Type											
		uint8_t		$uint16_t$		uint32_t			uint64_t				
		Total	Total	Average	Total	Total	Average	Total	Total	Average	Total	Total	Average
		Time	Energy	Power	Time	Energy	Power	Time	Energy	Power	Time	Energy	Power
Algorithm	Num Elements	(s)	(J)	(W)	(s)	(J)	(W)	(s)	(J)	(W)	(s)	(J)	(W)
Bubble Sort	50,000	5.53	66.66	12.03	5.39	65.29	12.09	5.66	69.05	12.19	5.78	71.83	12.41
Insertion Sort	200,000	7.98	102.18	12.75	7.98	103.00	12.85	7.46	98.81	13.21	7.54	105.03	13.89
Quicksort	2,000,000	5.51	61.73	11.20	5.53	61.90	11.19	5.52	61.60	11.15	5.51	62.90	$\star 11.42$
Merge Sort	60,000,000	•6.06	●72.33	11.93	6.07	72.46	11.93	6.12	75.65	12.36	•5.93	●76.98	$\star 12.98$
qsort	100,000,000	•5.84	72.39	12.37	6.15	76.90	12.48	6.79	86.29	12.69	●5.69	●73.25	12.86
Counting Sort	200,000,000	0.23	♦2.92	12.75	0.24	♦3.16	13.23	0.25	♦3.58	14.15	0.35	♦5.12	14.44

- Insertion Sort: 32 bit version more optimized
- Counting Sort:

75% more energy for 64 bit compared to 8 bit values

 Sorting 64 bit values takes less time than sorting 8 bit values, but consumed more energy

★ Average power variations between algorithms

EACOF on github: Get involved!

GitHub This repositor	y - Search or type a command	O Explore Fe	atures Enterprise Blog	Sign up Sign in
eacof / eacof				★ Star 4 \$2 Fork 0
The Energy Aware COmputir	ng Framework		A	<> Code
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Makefile	Release commit		13 hours ago	Clone in Desktop
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github.com/eacof

Static Analysis for Energy Consumption









Whole Systems ENergy TRAnsparency

EC FP7 FET MINECC:

"Software models and programming methodologies supporting the strive for the energetic limit (e.g. energy cost awareness or exploiting the trade-off between energy and performance/precision)."







Static Energy Usage Analysis

Original Program:

```
int fact (int x) {
    if (x<=0)<sup>a</sup>
        return 1<sup>b</sup>;
    return (x *<sup>d</sup> fact(x-1))<sup>c</sup>;
}
```

Extracted Cost Relations:

```
C_{fact}(x) = C_{a} + C_{b} \quad \text{if } x \leq 0

C_{fact}(x) = C_{a} + C_{c}(x) \quad \text{if } x > 0

C_{c}(x) = C_{d} + C_{fact}(x-1)
```

 Substitute C_a, C_b, C_d with the actual energy required to execute the corresponding lower-level (machine) instructions.



Energy Modelling

Energy Modelling

Energy Cost (E) of a program (P):

$$E_P = \sum_i (B_i \times N_i) + \sum_{i,j} (O_{i,j} \times N_{i,j}) + \sum_k E_k$$

Instruction Base Cost, B_i , of each instruction *i*

Circuit State Overhead, $O_{i,j}$, for each instruction pair Other Instruction Effects (stalls, cache misses, etc)

V. Tiwari, S. Malik and A. Wolfe. "Instruction Level Power Analysis and Optimization of Software", Journal of VLSI Signal Processing Systems, 13, pp 223-238, 1996.

XCore Energy Modelling

Energy Cost (E) of a multi-threaded program (P):

$$E_{\rm p} = P_{\rm base} N_{\rm idle} T_{\rm clk} + \sum_{t=1}^{N_t} \sum_{i \in \rm ISA} \left(\left(M_t P_i O + P_{\rm base} \right) N_{i,t} T_{\rm clk} \right)$$

Idle base power and duration

Concurrency cost, instruction cost, generalised overhead, base power and duration

- Use of execution statistics rather than execution trace.
- Fast running model with an average error margin of less than 7%

S. Kerrison and K. Eder, 2015. "Energy Modelling of Software for a Hardware Multi-threaded Embedded Microprocessor", ACM Transactions on Embedded Computing Systems (TECS). To appear.

The set up...



S. Kerrison and K. Eder, 2015. "Energy Modelling of Software for a Hardware Multi-threaded Embedded Microprocessor", ACM Transactions on Embedded Computing Systems (TECS). To appear.

ISA Characterization





Odd threads instruction (name & encoding)

ISA Characterization





ISA Characterization





ISA Characterization Insights

Is a*b = b*a?

Is a*b = b*a?



 $E(a*b) \neq E(b*a)$



W/A/B-Case Energy Consumption



Operand 2





Energy Consumption Analysis

Analysis at the ISA Level

- Combine static resource analysis (SRA) with the ISAlevel energy model.
- Provide energy consumption function parameterised by some property of the program or its data.



ISA-Level Analysis Results



U. Liqat, S. Kerrison, A. Serrano, K. Georgiou, N. Grech, P. Lopez-Garcia, M.V. Hermenegildo and K. Eder. "Energy Consumption Analysis of Programs based on XMOS ISA-Level Models". LOPSTR 2013.

Analysis Options



- Moving away from the underlying model risks loss of accuracy.
- But it brings us closer to the original source code.

Mapping LLVM IR to Assembly

LLVM-IR	ISA				
LoopBody: %deref1 = load i32* %i store i32 %deref1, i32* % br label %LoopTest2, ldbg LoopBody3: %3 = load i32* %numbers.bound %deref6 = load [0 x i32]** %numbers %deref7 = load i32* %j %boptmp8 = sub i32 %deref7, 1 %subscript = getelementptr [0 x i32]* %deref6, i32 0, i32 %boptmp8 %deref9 = load i32* %subscript %4 = load i32* %numbers.bound %deref10 = load [0 x i32]** %numbers %deref10 = load [0 x i32]** %numbers %deref11 = load i32* %j %subscript12 = getelementptr [0 x i32]* %deref10, i32 0, i32 %deref11 %deref13 = load i32* %subscript12 %relopcmp = icmp sgt i32 %deref9, %deref13 %cast = zext i1 %relopcmp to i32 %zerocmp = icmp ne i32 %cast, 0 bel %feref1 %	.label10 0x000100da: 05 5c: ldw (ru6) r0, sp[0x5] 0x000100dc: 04 54: stw (ru6) r0, sp[0x4] 0x000100de: 20 73: bu (u6) 0x20 <.label5> .label8 0x000100e0: 08 5c: ldw (ru6) r0, sp[0x8] 0x000100e2: 44 5c: ldw (ru6) r1, sp[0x4] 0x000100e2: 44 5c: ldw (ru6) r1, sp[0x4] 0x000100e4: 21 f8 ec 1f: ldaw (l3r) r2, r0[r1] 0x000100e8: 68 9a: sub (2rus) r2, r2, 0x4 0x000100ea: 28 08: ldw (3r) r0, r0[r1] 0x000100ee: 02 c0: lss (3r) r0, r0, r2 0x000100ee: 02 c0: lss (3r) r0, r0, x14 <.label6> 0x000100f2: 00 73: bu (u6) 0x0 <.label7>				
br 11 %zerocmp, label %iftrue, label %ifdone					

K. Georgiou, S. Kerrison and K. Eder, 2015. "A Multi-level Worst Case Energy Consumption Static Analysis for Single and Multi-threaded Embedded Programs", ACM Transactions on Architecture and Code Optimization (TACO). To be submitted; draft available on request.

Analysis at the LLVM-IR Level



WCEC Static Analysis Results



submitted; draft available on request.

Towards Energy Aware Software Engineering



- For HW designers: "Power is a 1st and last order design constraint." [Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]
- "Every design is a point in a 2D plane."

[Mark Horowitz, E³S 2009]



Scaling Power and the Future of CMOS

Mark Horowitz, EE/CS Stanford University



- For HW designers:
 "Power is a 1st and last order design constraint."
 [Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]
- "Every design is a point in a 2D plane."

[Mark Horowitz, E³S 2009]

Optimizing Energy



18



- For HW designers: "Power is a 1st and last order design constraint." [Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]
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Optimizing Energy



Performance



- For HW designers: "Power is a 1st and last order design constraint." [Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]
- "Every design is a point in a 2D plane."

[Mark Horowitz, E³S 2009]

Optimizing Energy



20

Optimizing Energy

More POWER to SW Engineers

in 5pJ do {...}

- Full Energy Transparency from HW to SW
- Location-centric programming model

- "Cool" code
 - A cool programming competition!

Promoting energy efficiency to a 1st class SW design goal is an urgent research challenge.











EACO @ Bristol

The Energy-Aware COmputing Initiative, Research Agenda and Workshops

http://www.cs.bris.ac.uk/Research/Micro/eaco.jsp

EACO Research at Bristol



- EACO Platform
 - Online power monitoring
 - RTOS API
- EACOF (<u>github.com/eacof</u>)
 - API for SW energy measurement
- Machine Guided Energy Efficient Compilation (MAGEEC)
- Superoptimization for low energy
- Whole Systems Energy Transparency (ENTRA)











lome Project Consortium News Events Publications Contacts Login



Welcome to the ICT-Energy project website!

The goal of the project is to create a coordination activity among consortia involved in the ICT-Energy field with specific reference to bringing together the existing "Toward Zero-Power ICT" community organized within the ZEROPOWER project and the novel "MINECC" (Minimising energy consumption of computing to the limit) community recently funded under the FET Proactive Call 8 (FP7-ICT-2011-8) Objective 9.8. The coordination activity is aimed at assessing the impact of the research efforts developed in the groups involved in the different consortia and proposing measures to increase the visibility of ICT-Energy related initiatives to the scientific community, targeted industries and to the public at large through exchange of information, dedicated networking events and media campaigns.

Please visit the website to stay informed on our news and initiatives. We hope you find the information in this website interesting and stimulating. If you want to know more about the project or its topic, please do not hesitate to contact us.

L E T F R ICT-ENERGY New condition action and glub 2EROPOWER and MINECC communities. GALILEO The French – Italian colladoration in the project Galibon. NANOPOWER The excellent results of the Emogeneous research project ENTRA and LANDAUER Project news. Scientific papers The section of ICT- ENREGIETETER decoded by contributed 2pro ZHE LANDAUER Project news.	NERGY		[–]E	ICI
ICT-ENERGY GALILEO NANOPOWER ENTRA and Scientific papers ZEE New conditation action among he ZEROPOWER and MINECC communities. The French – Iulian collaboration in the project factors The section of ICT- the European research project The section of ICT- project nees. The section of ICT- Project nees. The ENERGY IETTERS Agen Accord to contributed The	T E R S	r r	I	L E
NANOPOWER manuscripts.	NOPOWER wedlent results of unpoan research i ENTRA and LANDAUER Project news. Scientific papers The section of ICT- ENERGY LETTERS decoted is contributed manuacripts. ZEROPOWER The Statigie Research Agenda "Towards Zero-Power ICT".	NANOPOWER The excellent results of the European research project NANOPOWER.	GALILEO The French – Italian collaboration in the project Galiko.	ICT-ENERGY New coordination action among the ZEROPOWER and MINECC communities.

NANOENERGY Letters becomes ICT-ENERGY Letters. The change in name reflects our intention to keep our promise to become the scientific journal of a rapidly growing community interested in the various aspects associated with the role of energy in Information and Communication Technology. In this issue, as it is customary, we present some news together with scientific articles and documents. On the news side we report on the conclusion of the

report on the EC funded 3-year action (c.a.) ZEROPOWER. In novel c.a. ICTwww.ict-energy.eu) role of promoting field and we emergence of this welcoming in our



representatives from the various consortia involved in the c.a. ICT-Energy. It is worth mentioning that in this issue we publish the updated version of the ZEROPOWER Strategic Research Agenda. This is an important document that has the ambition to help defining the state of the art of the research in this field and to draw the lines for future developments. Finally I would like to mention the recent publication of the new science book entitled *ICT-Energy. Concepts Towards Zero - Power Information and Communication Technology.* This is freely available for download at the INTECH web site: http://www.intechopen.com/books. (LG)

This newsletter is edited with the
collaboration of the ICT-ENERGY
editorial board composed by:

- L. Gammaltoni, NIPS Laboratory, University of Perugia (IT)
- L. Worschech, University of Wuerzburg (DE)
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- Barcelona (ES)
- F. Marchesoni, University of Camerino (11)
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 inoma de Barcelona (ES)
- P. Douglas, University of Glasgow (UK)

coordination

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Energy

editorial

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- K. Ed er, University of Bristol (UK)
- K.G.Larsen, Aalborg Universitet (DK)

http://www.ict-energy.eu/

University of BRISTOL

Energy Aware COmputing (EACO) research at the UNNERSITY OF BRISTOL includes both Computer Science and Electronic Engineering, with significant cross-departmental expertise and collaboration in energy monitoring and modelling, static analysis and compilers, processor architectures and embedded multi-core system design. The EACO Workshop series at the Univenity of Bristol brings together academia and industry to identify and address intellectual challenges in Energy Aware Computing with the aim to reduce the energy cosumption of computation. Topics of EACO Workshops span the entire system stack from application software and algorithms, via programming language, compilers, operating systems, instruction sets and micro architectures to the design of hardware.

University of Bristol contact: Kerstin Eder



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Coordinating research efforts towards

LOW ENERGY ICT

The goal of the ICT-Energy project is to create a coordination

activity among researchers working on energy reduction in ICT from

Nanoscale Devices to Exascale Computing

By bringing together the Toward Zero-Power ICT community with

the MINECC (MINimizing Energy Consumption of Computing)

community this project enables a concerted effort to lower energy

consumption across the ICT sector.

Our aim is to assess the impact of existing research efforts and

propose measures to increase the visibility of ICT-Energy related

initiatives to the scientific community, targeted industries and to

the public at large through the exchange of information, dedicated

networking events, education and media campaigns.

www.ict-energy.eu

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The UNIVERSITY OF GLASGOW's James Watt Nanofabrication Centre use micro- and nano-technology research and manufacturing facilities to develop technology including Terahertz optics and Silicon nano-wirres, healthcare applications and emergy harvesting. The Centre coordinates the Generate Renewable Energy Efficiently using Nanofabricated Silicon (GREEN Silicon) project, where the Seebeck effect is used to produce thermoelectric generators using Si/SiGe heterolayer technology, resulting in more efficient energy harvesting.

University of Glassow contact: Douglas Paul

Tyndall

TYNDALL NATIONAL INSTITUTE is one of Europe's leading centres in ICT research and development. Applying an "atoms to systems" philosophy, energy research in Tyndall includes advanced concepts for low-power computing and efficient power supplies, energy storage and harvesting solutions, and technologies for wireless. sensor networks applied to energy and resource optimisation in buildings and factories.
Tyndall coordinates a number of projects in the ICT-Energy field including the MANPOWER, SINAPS, SUWIRE, PowerSWIPE and DEEPEN projects.
Tyndall National Handmacontas: Groups Pages

> coordinator: Prof. Luca Gammaltoni NPS Laboratory, Dipartimento di Fisica Università di Perugia Via A. Pascoli, 1 - 06123 Perugia, Italy telephone: +39-0755852733 (az: +39-0755846458

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The UNIVERSITY OF PERUGIA's Note in Physical Systems (NIPS) Lab studies the effects of fluctuations in electrical fields, heat, sound and other mediums. This has led to the development of novel energy harvesting and notes sensing devices. The NIPS Laboratory coordinates the LANDALER project where the operation of basic physical switches below the Landauer limit is studied to investigate conceptually new devices and novel computing paradigms with radically improved power efficiency. Deverte of Provide conjuil: tas Generaled



ROSPLDE UNIVERSITY's Programming, Logic and intelligent Systems (PLUS) group focus on the theoretical aspects of programming languages and their applications. PLIS has significant expertise in software verification, program analysis and transformation.

The PLES group coordinates the Whole Systems Energy Transparency (ENTRA) project where advanced program analysis and energy modelling techniquess are used to predict the energy consumption of programs early on during software development. This enables energy-aware software engineering.



The UNIVERSITY OF HEIDELBERG's Engineering Mathematics and Computing Lab (IMAC) applies numerical analysis to optimise the performance and energy consumption of High Performance Computing (IPC) as used in leading edge scientific programming. The EVACL coordinates the EXAZOREN project which aims to drastically reduce the energy consumed in HPC by developing advanced power consumption monitoring and profiling, and designing a smart, power-aware scheduling technology for HPC. University of Medicing corect: Vocat TexaNets



At the HITACHI CAMBRIDGE LABORATORY (HCL) researchers investigate new designs of micro and optoelectronic devices, based on entirely new concepts, such as single electron logic circuits. Revolutionising the electronic devices used to power information technology has the potential to cut energy consumption by orders of magnitude. EICL coordinates the Towner Low Power ICT (TOLOP) project which aims at the renitzation of novel low power devices (single electron transistors and single atom transitors), including implementation theory and the corresponding design architectures. EICL energy and the corresponding design architectures.



arcelona apercomputing anter nto Ascions de Supercomp

BARCELONA SUPERCOMPUTING CENTER (IBC) uses HPC expertise to develop entirely new system-architecture models for 100-energy HPC. The BSC coordinates the Parallel Distributed Infrastructure for Minimization of Energy (ParaDNE) project where radical software-hardware co-design techniques are being developed that are driven by future device characteristics on one side, and by a programming model based on message passing on the other side. This approach is expected to yield dramatic energy simings in heterogeneous distributed systems.

BSC contact: Adrián Cristal Sertelman



ALBORG UNIVERSITY's Center for Embedded Software Systems (CISS) improve embedded systems development through the use of model-driven design tools. These allow designs to be written in a verifiable way, and analyzed for energy consumption and performance. The CISS coordinates the Set Forengy-Supporting Autonomous Computation (SENSATION) project which aims at increasing the scale of systems that are self-supporting by balancing energy barvestion and consumetion. The mesonch addresses the challence

harvesting and consumption. The research addresses the challenge of programming systems that reconfigure themselves in response to changing tasks, resources, errors and available energy.

Asiborg University contact: Rim Goldstrand Lamon



ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSAMIE (EPFL) specialise in embedded and low-power systems, efficiently designed software algorithms and system level optimisations. EPFL coordinates the PHDIAS project which proposes the development of an ultra-low power smart bio-sensing wireless body sensor network, making use of new signal processing models and methods for efficient data handling. This enables long term low energy monitoring of bio-signals.

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Thank you for your attention





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