Energy Transparency from Hardware to Software

Why SW engineers are key to energy efficient computing

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Free mobile apps 'drain battery faster'

Free mobile apps which use third-party services to display advertising consume considerably more battery life, a new study suggests.

Researchers used a special tool to monitor energy use by several apps on Android and Windows Mobile handsets.

Findings suggested that in one case 75% of an app's energy consumption was spent on powering advertisements.

Like many games, Angry Birds has a free version supported by targeted advertising

Report author Abhinav Pathak said app makers must take energy optimisation more seriously.

Energy Aware System Design

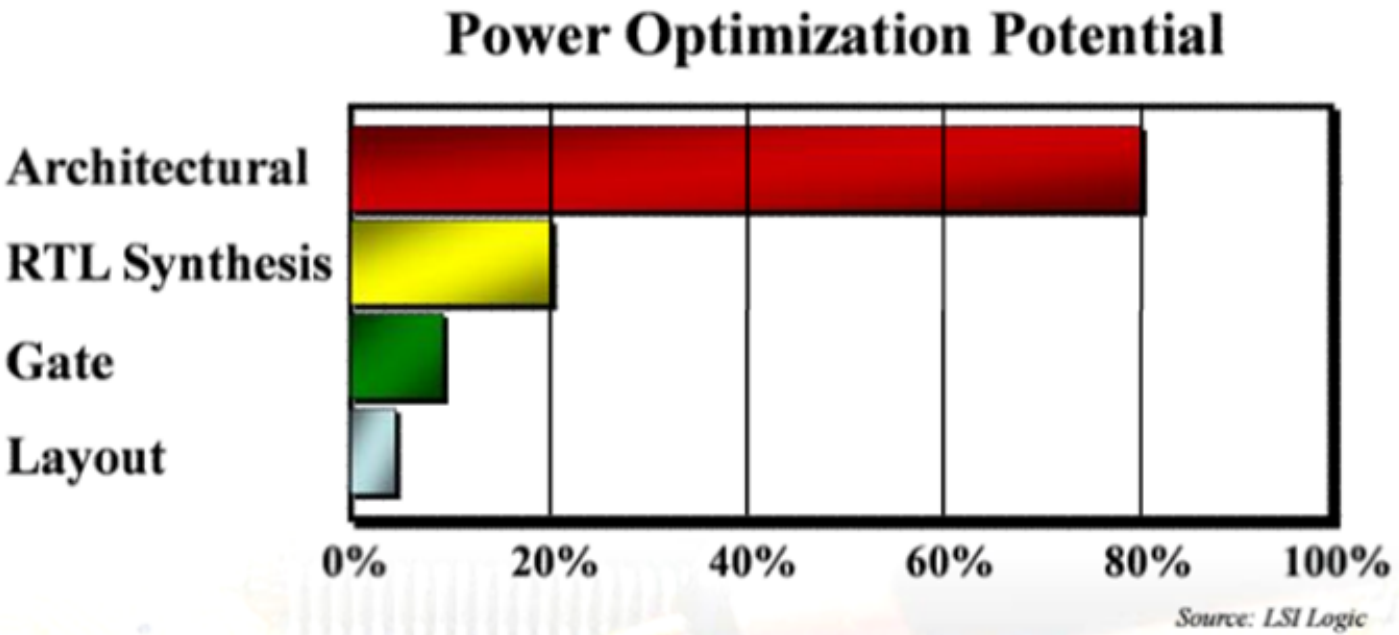
Hardware Design

- Power management largely in domain of Hardware Design
  - Considerations to minimize/optimize
    - Dynamic (switching) and static (leakage) power
  - On-chip power management
    - Modes: on, standby, suspend, sleep, off
- Development of low power electronics

Where can the greatest savings be made?

Greater Savings at Higher Levels

Why Optimize Power at the Architecture?



LOW POWER

Lack of software support marks the low power scorecard at DAC

One of the panels at the Design Automation Conference (DAC), which took place in California in early June, set out to get an idea of how well the industry is doing at delivering lower-power systems.

It is becoming clear, *writes Chris Edwards*, that the system level is currently the missing link.

Processes can deliver some gains – and Globalfoundries' Andrew Brotman was able to outline some of the features that the foundry has put into its recently launched low-power high-k, metal gate (HKMG) process.

FinFETs should bring power down as those processes become available, although they are not the only options. But if the software keeps cores active for no good reason, the lower switching power per bit processed won't deliver a realised saving.

In his keynote speech Gadi Singer, vice-president IAG and general manager of the SoC enabling group at Intel Corporation, said that with limited software support, dedicated low-power circuitry could save maybe 20% in a typical multimedia-oriented core.

Make the software controlling it better at controlling the power states and that difference could be three to five times.

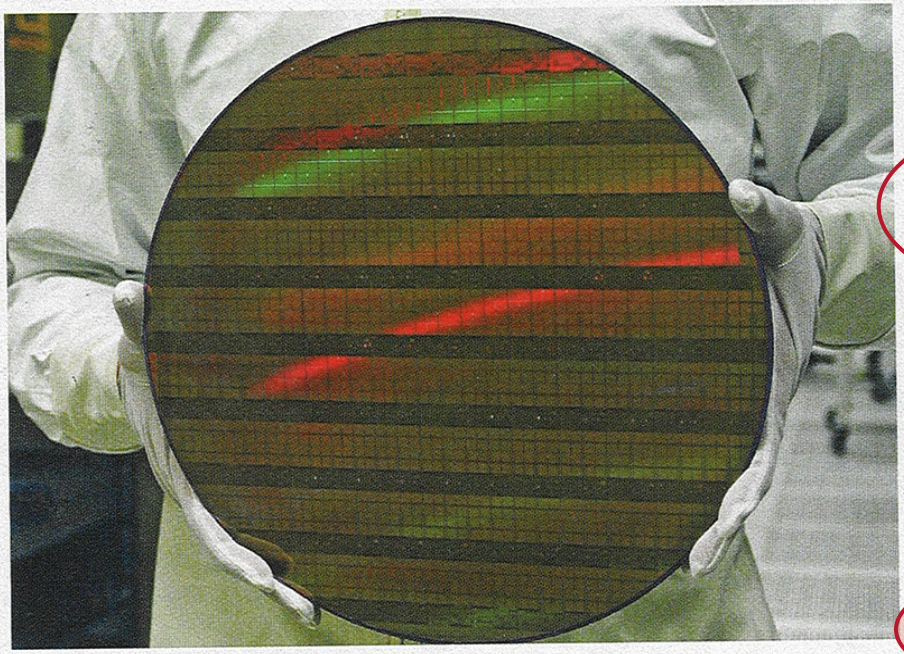
During an afternoon panel discussion Ambrose Low, director of design engineering at Broadcom said: "We have hundreds of knobs in the hardware to turn power down.

"The question is whether we can take the actual use-cases into consideration and optimise the software to power the logic circuits down. We still have a long way to go."

Ruggero Castagnetti of LSI argued that the desire to do more in software will grow.

"As we see power limits and targets becoming unachievable, customers will be willing to go to that extra step. There is a challenge that needs to be addressed and we have to do more on the systems side," Castagnetti said.

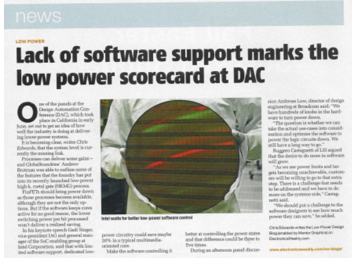
"We should put a challenge to the software designers to see how much power they can save," he added.



Intel waits for better low-power software control

Chris Edwards writes the Low-Power Design Blog (enabled by Mentor Graphics) on ElectronicsWeekly.com

www.electronicsweekly.com/ew-blogs/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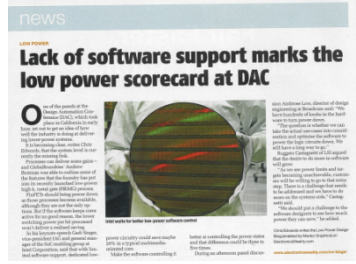
Wasted Potential

Huge advances have been made in power-efficient hardware.

BUT – potential energy savings are wasted by

- software that does not exploit energy-saving features of hardware;
- poor dynamic management of tasks and resources.

The Focus is on Software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Lack of software support marks the low power scorecard at DAC

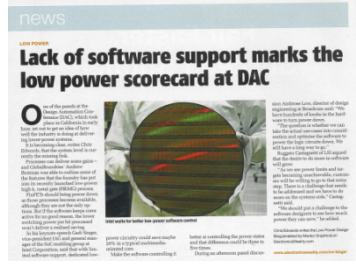
- Software controls the behaviour of the hardware
  - Algorithms and Data Flow
  - Compiler (optimizations)
    - Traditional SW design goals:

      performance,

      performance,

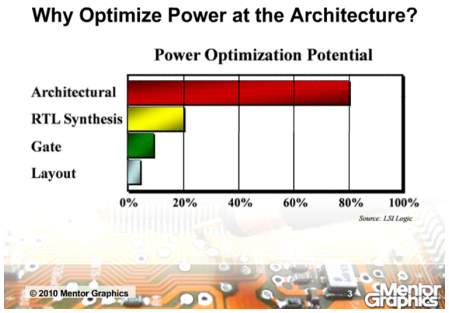
      performance

The Focus is on Software


news

Lack of software support marks the low power scorecard at DAC

- Software engineers often **"blissfully unaware"**
  - Implications of algorithm/code/data on power/energy?
  - Power/Energy considerations
    - at best, secondary design goals
- BUT the **biggest savings** can be gained from optimizations at the higher levels of abstraction in the system stack
  - Algorithms,
  - Data and
  - SW



6.3. SOFTWARE DESIGN FOR LOW POWER

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School of Electrical and Computer Engineering
Purdue University
West Lafayette, Indiana, U.S.A.

1. Introduction

It is tempting to suppose that only hardware dissipates power, not software. However, that would be analogous to postulating that only automobiles burn gasoline, not people. In microprocessor, micro-controller, and digital signal processor based systems, it is software that directs much of the activity of the hardware. Consequently, the software can have a substantial impact on the power dissipation of a system. Until recently, there were no efficient and accurate methods to estimate the overall effect of a software design on power dissipation. Without a power estimator there was no way to reliably optimize software to minimize power. Since 1993, a few researchers have begun to crack this problem. In this chapter, you will learn

Aligning SW Design Decisions with Energy Efficiency as Design Goal

Key steps*:

- *"Choose the **best algorithm** for the problem at hand and make sure it **fits well with** the computational **hardware**. Failure to do this can lead to costs far exceeding the benefit of more localized power optimizations.*
- *Minimize **memory size** and expensive **memory accesses** through algorithm transformations, efficient mapping of data into memory, and optimal use of memory bandwidth, registers and cache.*
- *Optimize the **performance** of the application, making **maximum use of available parallelism.***
- *Take advantage of **hardware support for power management**.*
- *Finally, select instructions, sequence them, and order operations in a way that **minimizes switching** in the CPU and datapath."*

* Kaushik Roy and Mark C. Johnson. **1997**. "Software design for low power". In *Low power design in deep submicron electronics*, Wolfgang Nebel and Jean Mermet (Eds.). Kluwer Nato Advanced Science Institutes Series, Vol. 337. Kluwer Academic Publishers, Norwell, MA, USA, pp 433-460.

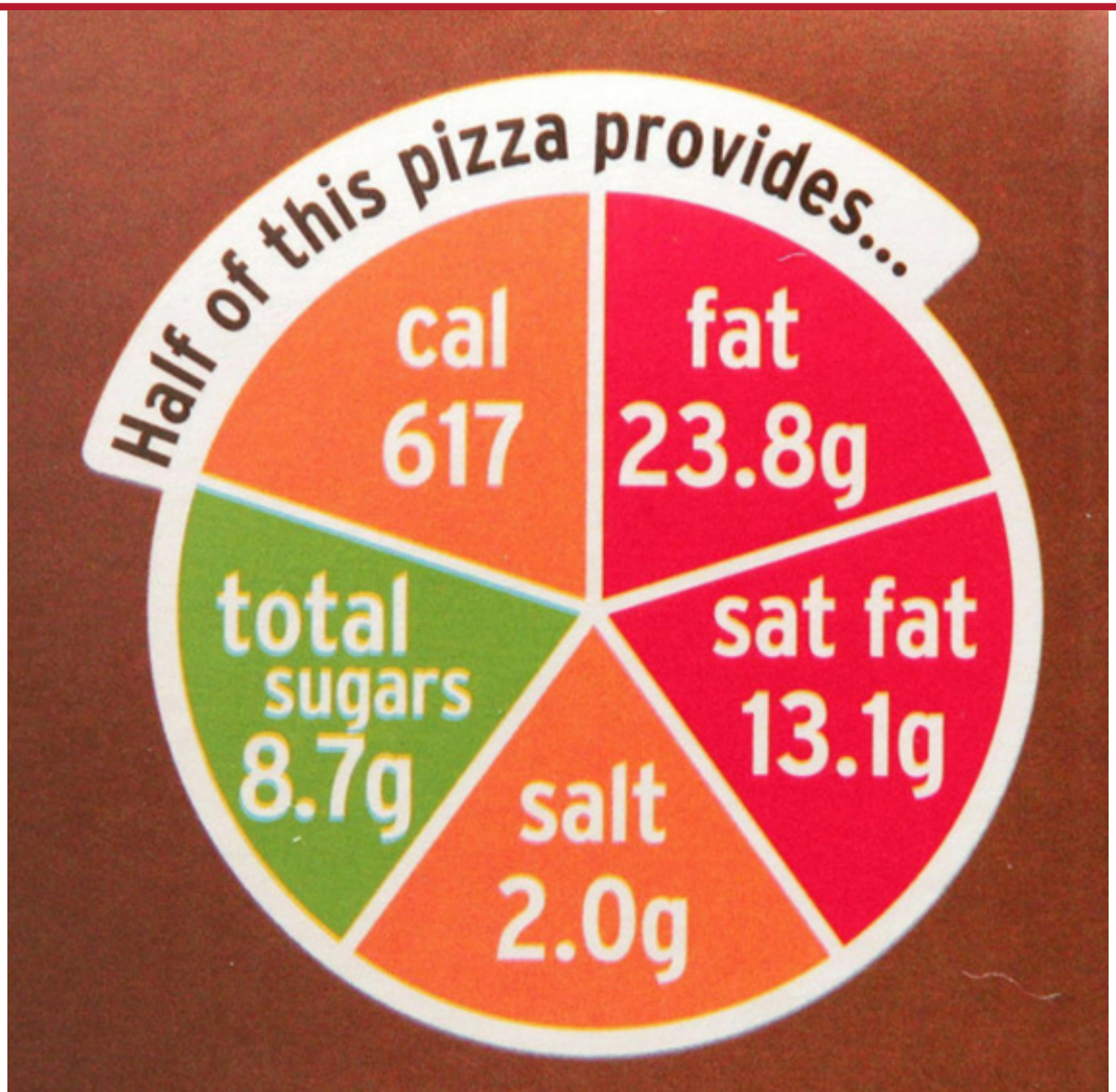
Energy Transparency

Energy Transparency

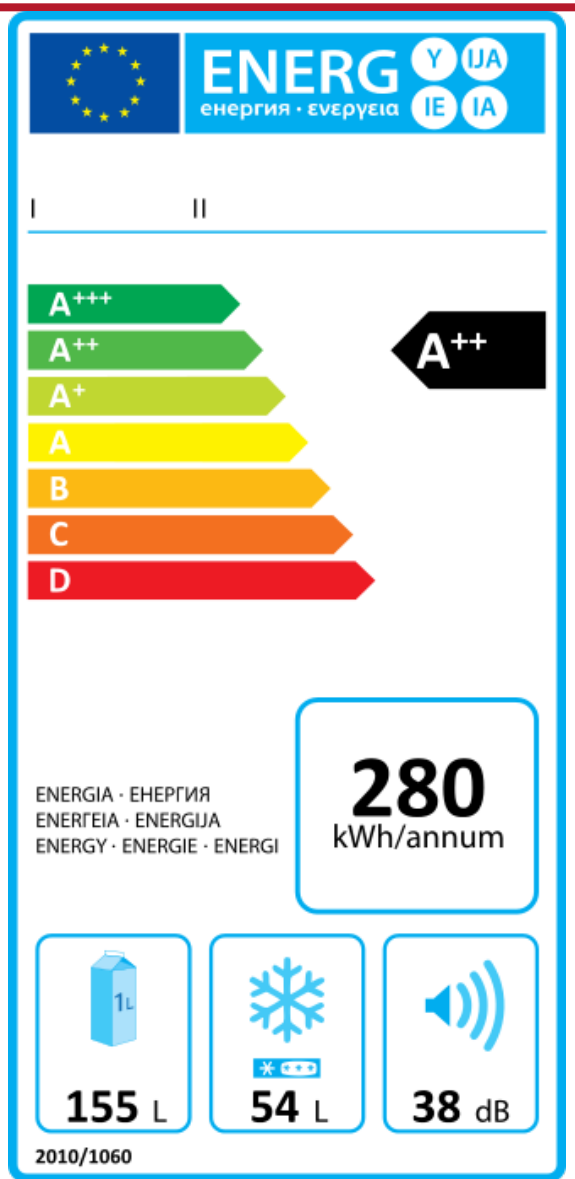
Information on energy usage is available for programs:

- ideally without executing them, and
- at all levels from machine code to high-level application code.

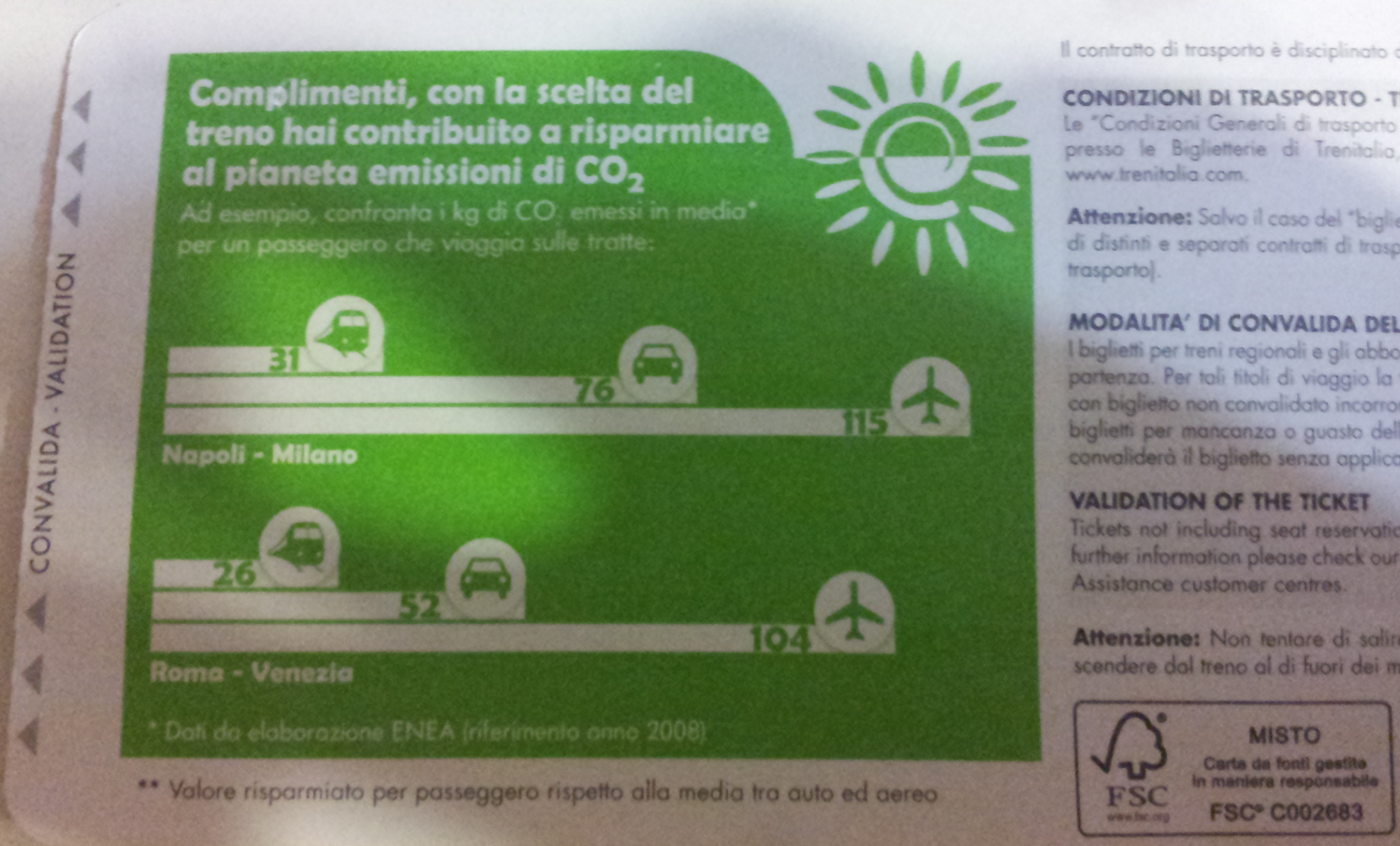
Transparency



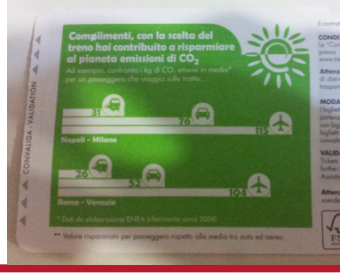
Transparency



Transparency

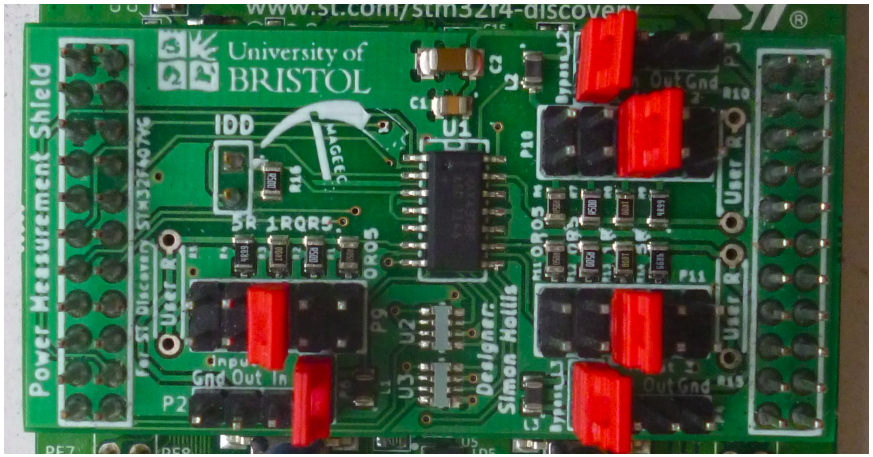


Why Energy Transparency?

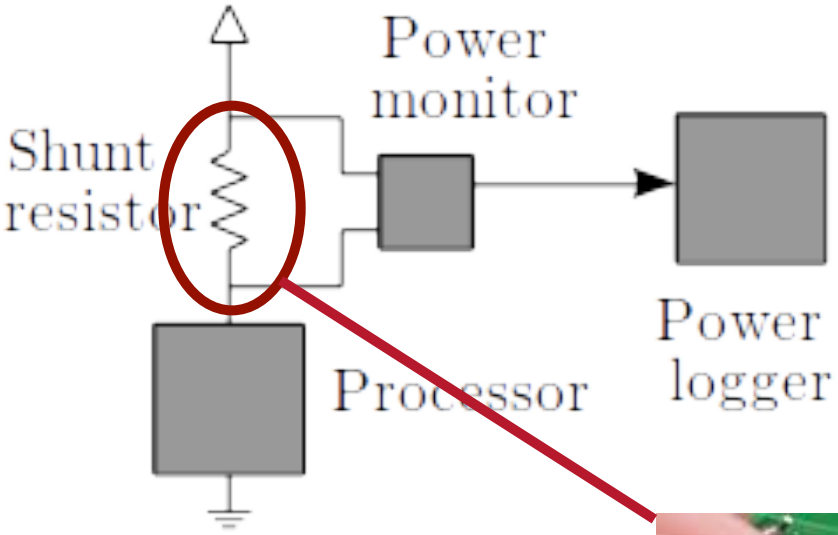


Energy transparency enables a deeper understanding of how algorithms and coding impact on the energy consumption of a computation when executed on hardware.

Measuring the Energy Consumption of Computation



The Showstopper ☹



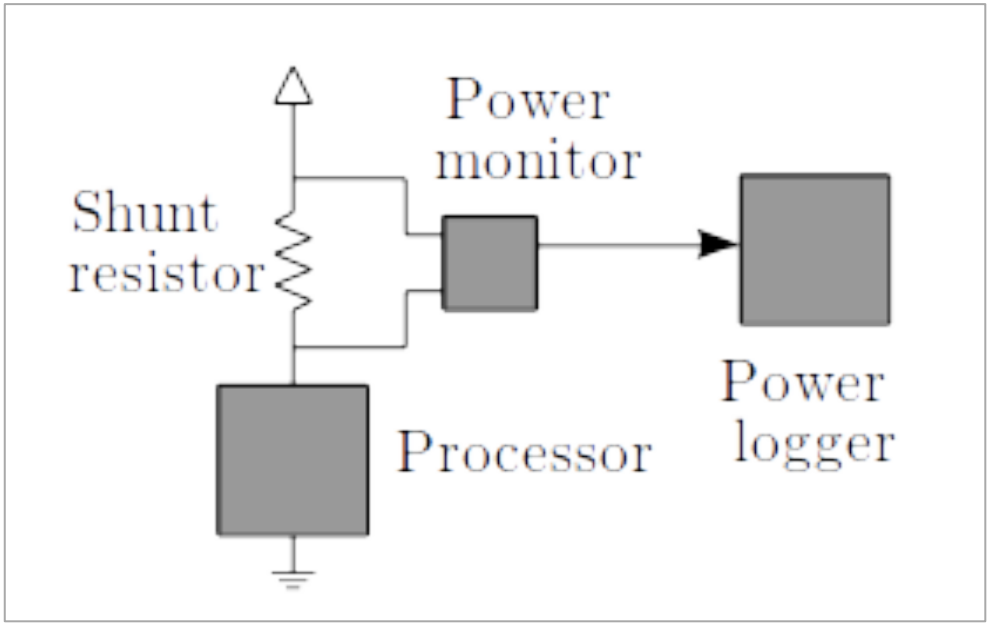
Measuring Power

Measure voltage drop across the resistor

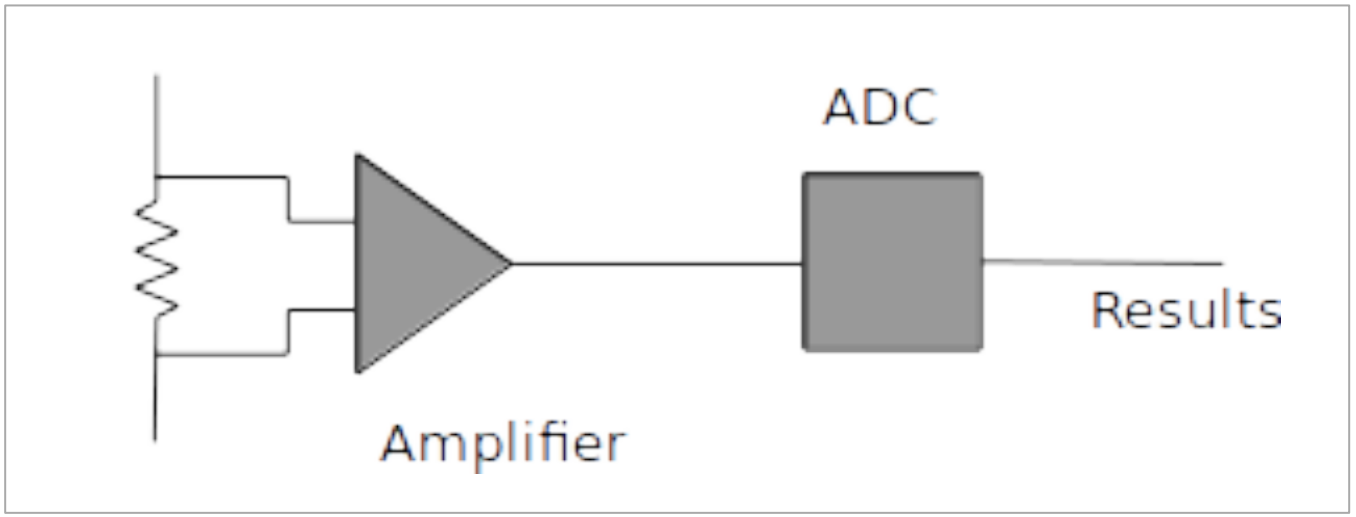
I = Vshunt / Rshunt to find the current

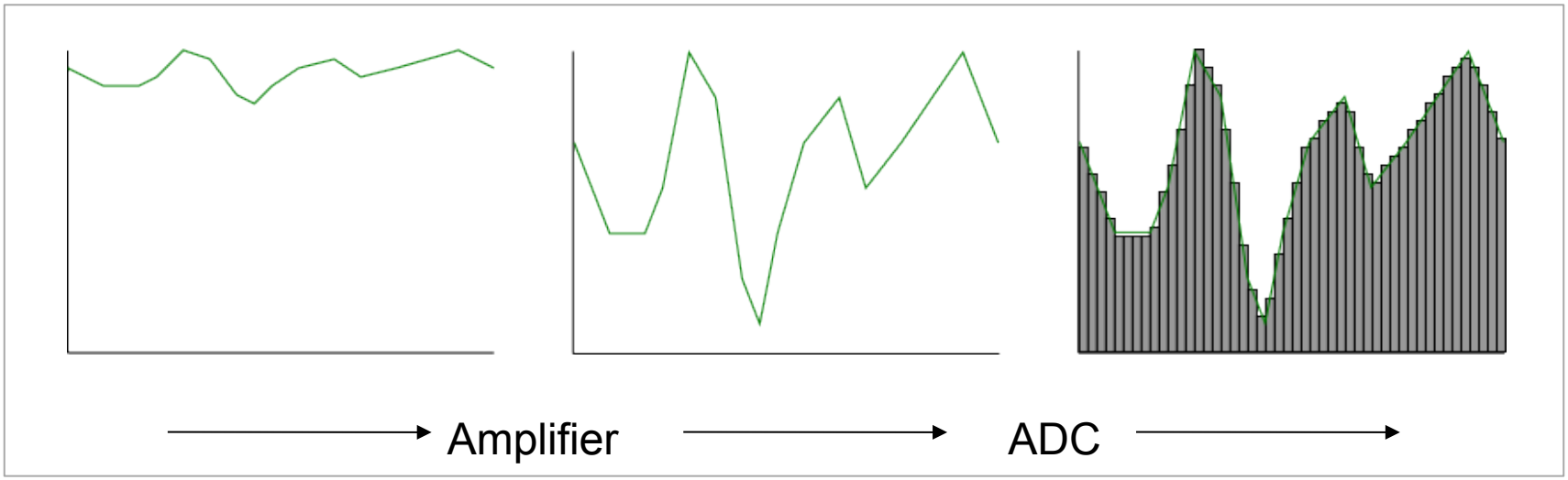
Measure voltage at one side of the resistor

P = I × V to calculate the power



The Power Monitor





Measuring Power

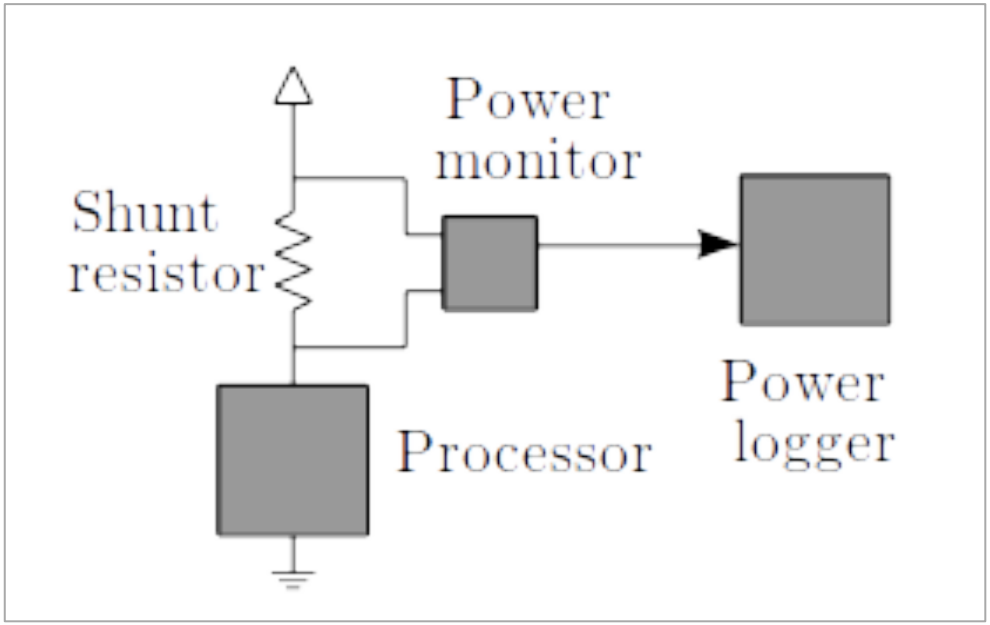
Repeat frequently, timestamp each sample

Measure voltage drop across the resistor

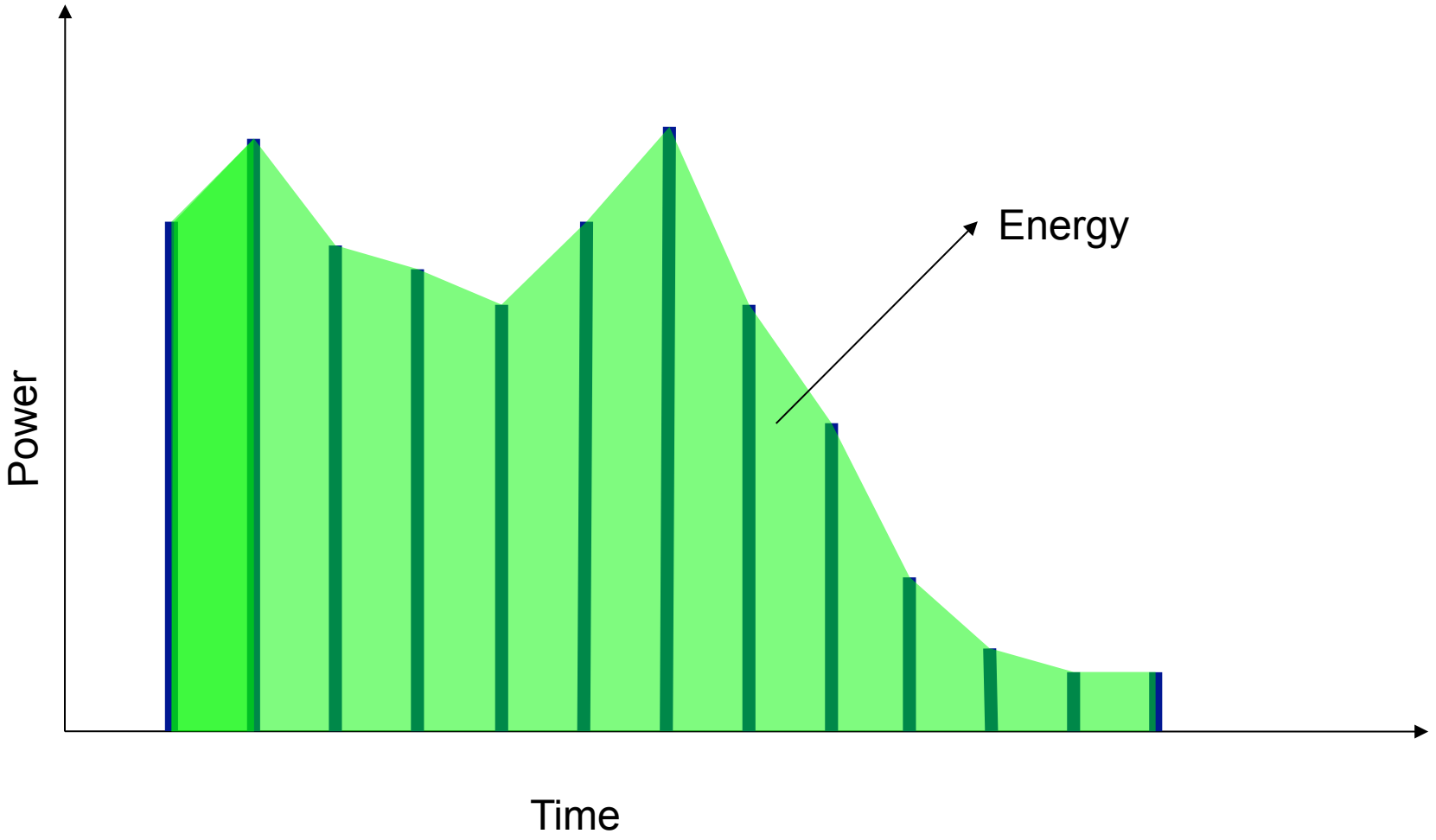
I = Vshunt / Rshunt to find the current

Measure voltage at one side of the resistor

P = I × V to calculate the power



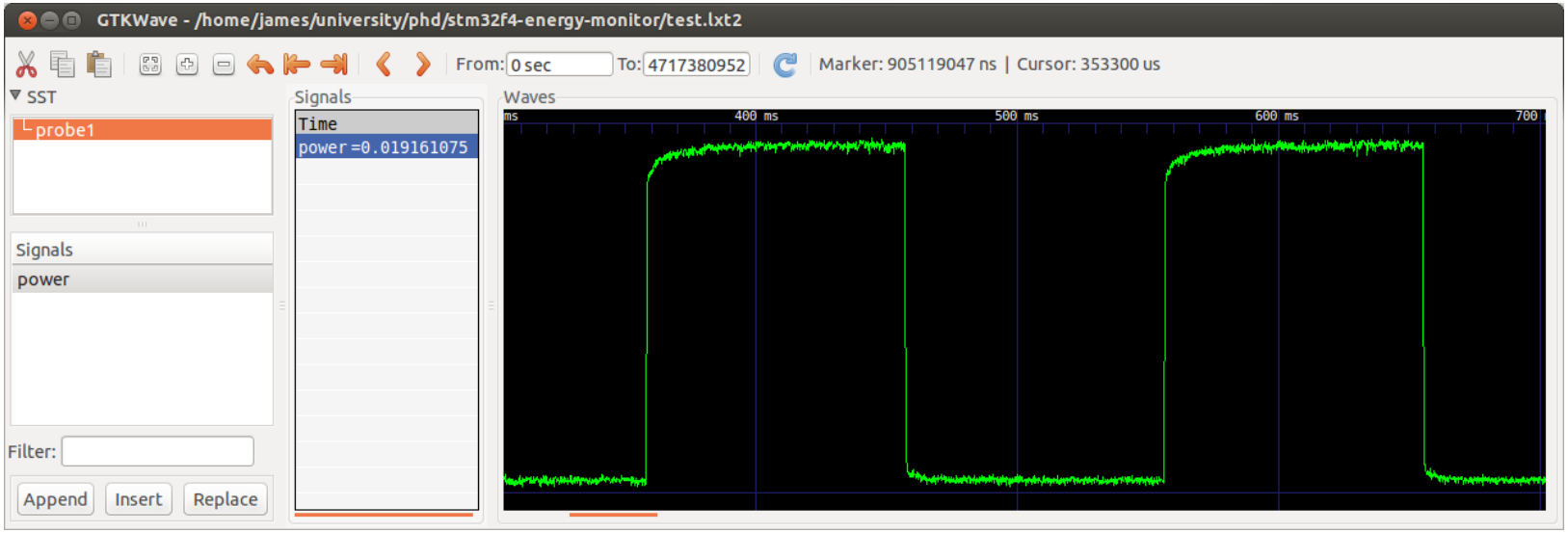
Measuring Energy



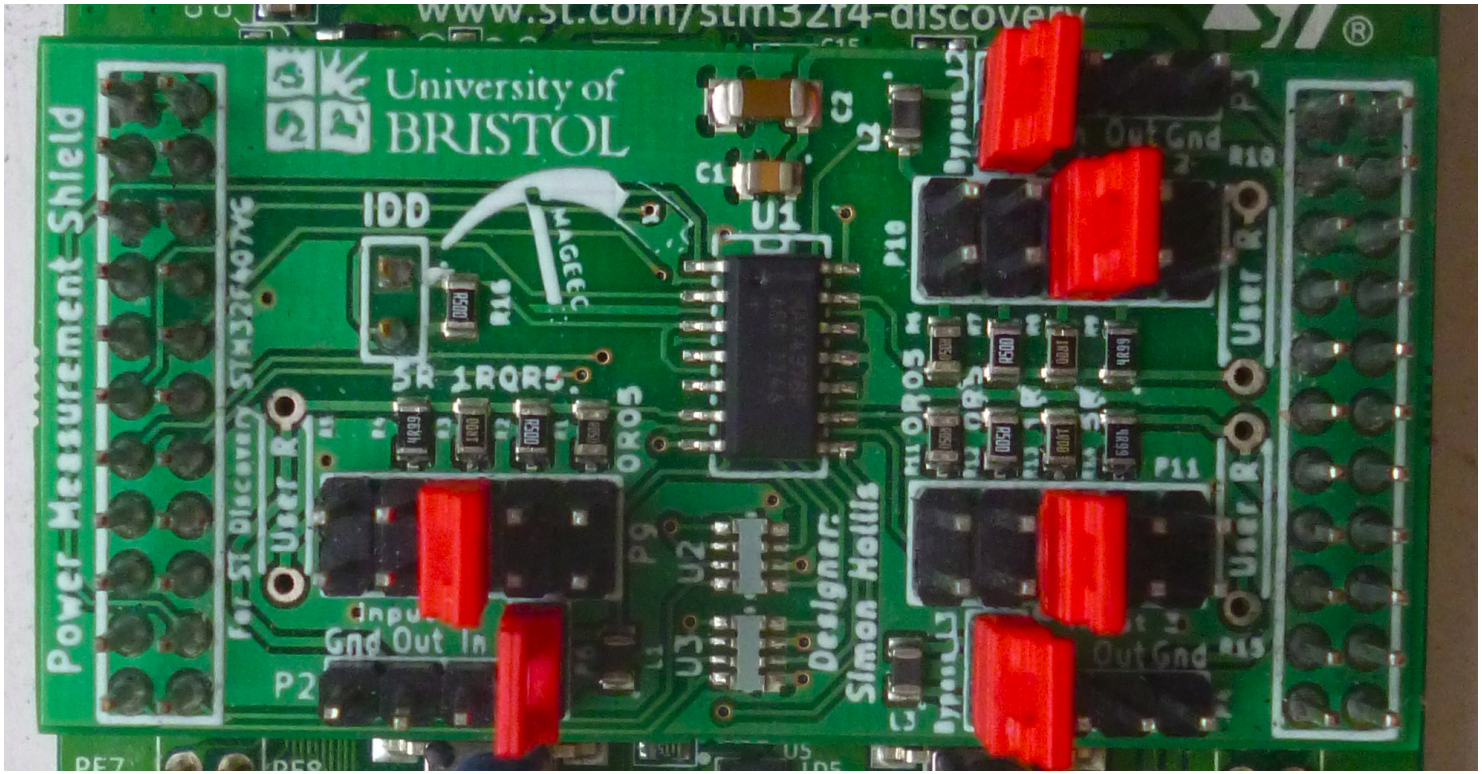
How much data?

Currently 500,000 Samples/second

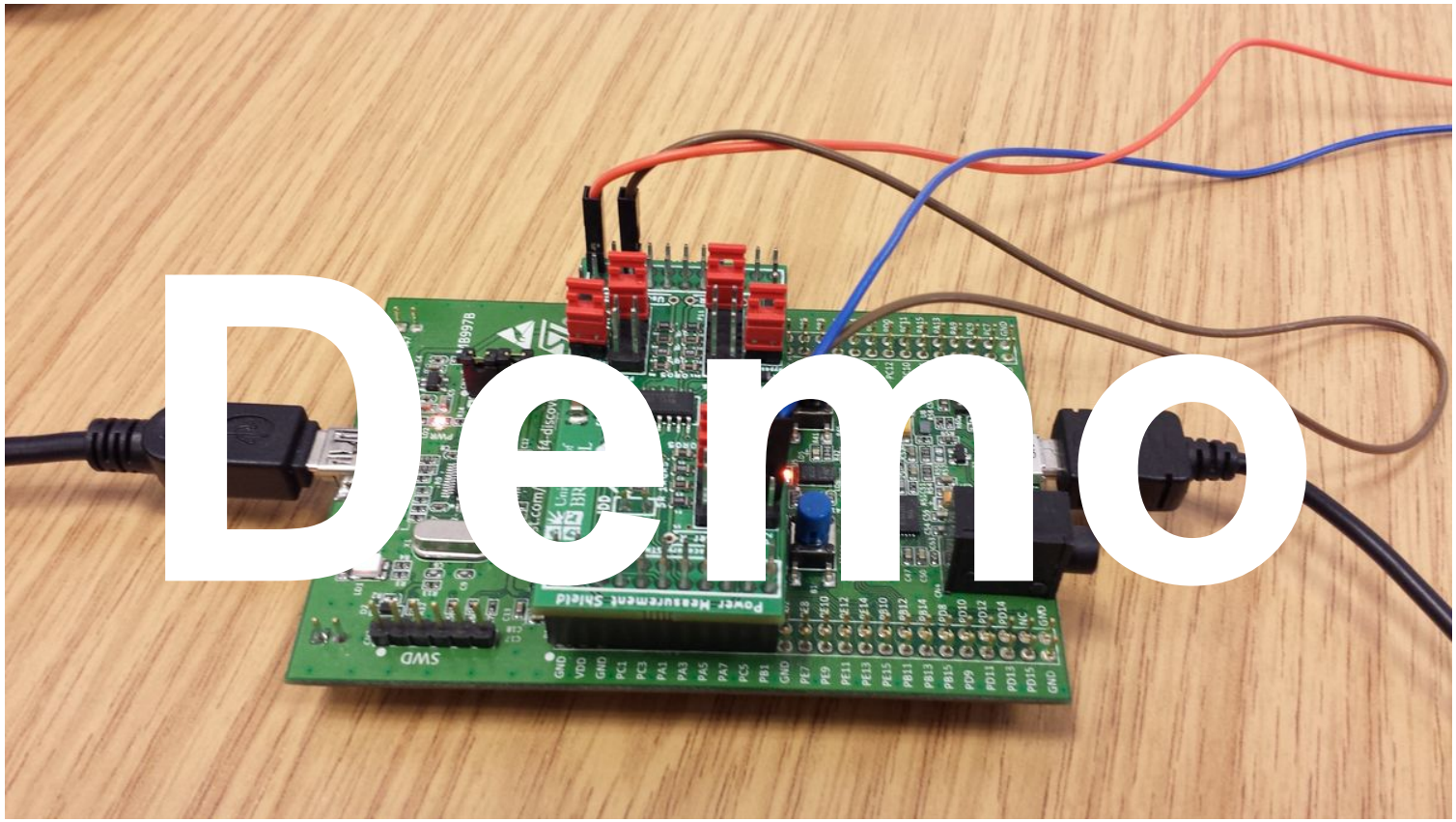
6,000,000 S/s possible in bursts



Open Energy Measurement Board



Energy Measurement



Online Demo

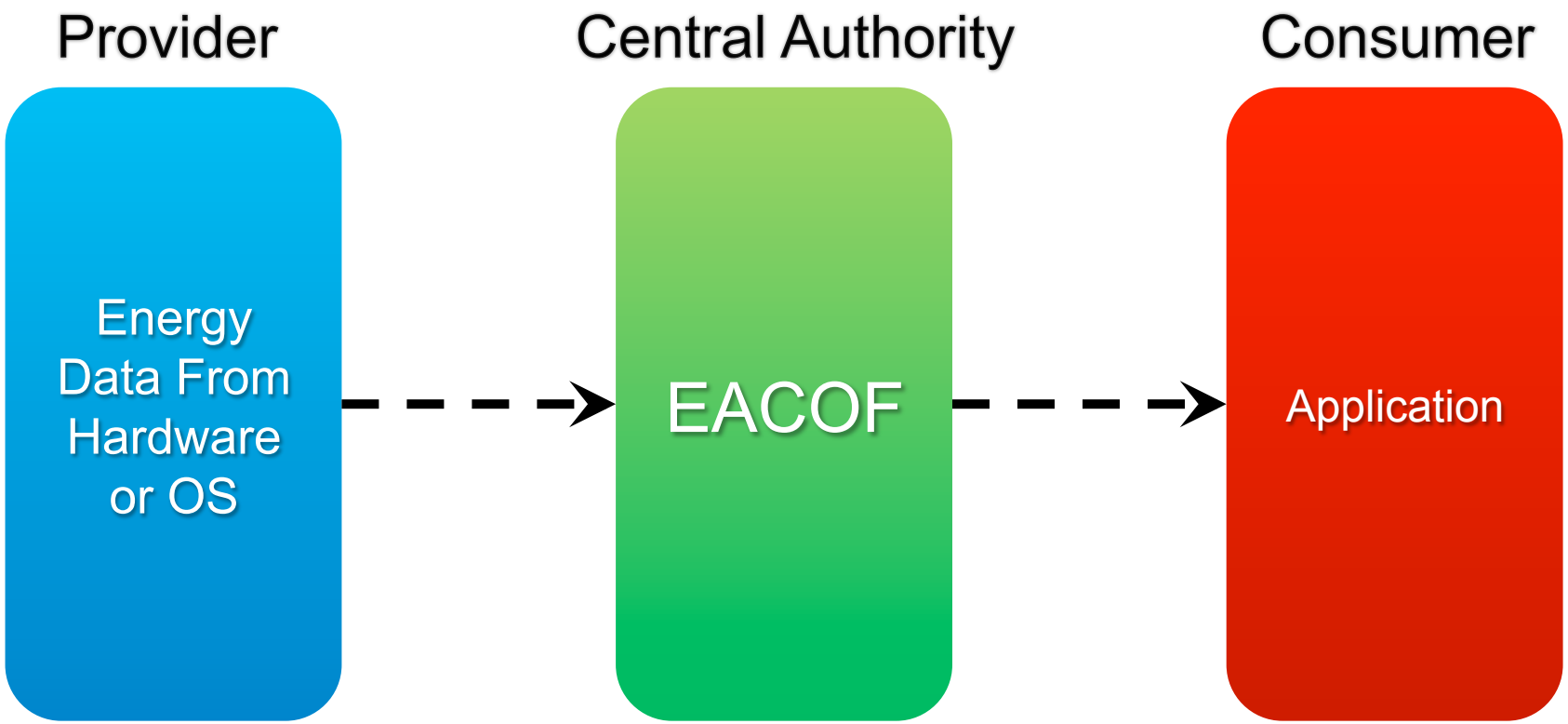
Dynamic Energy Monitoring

The EACOF

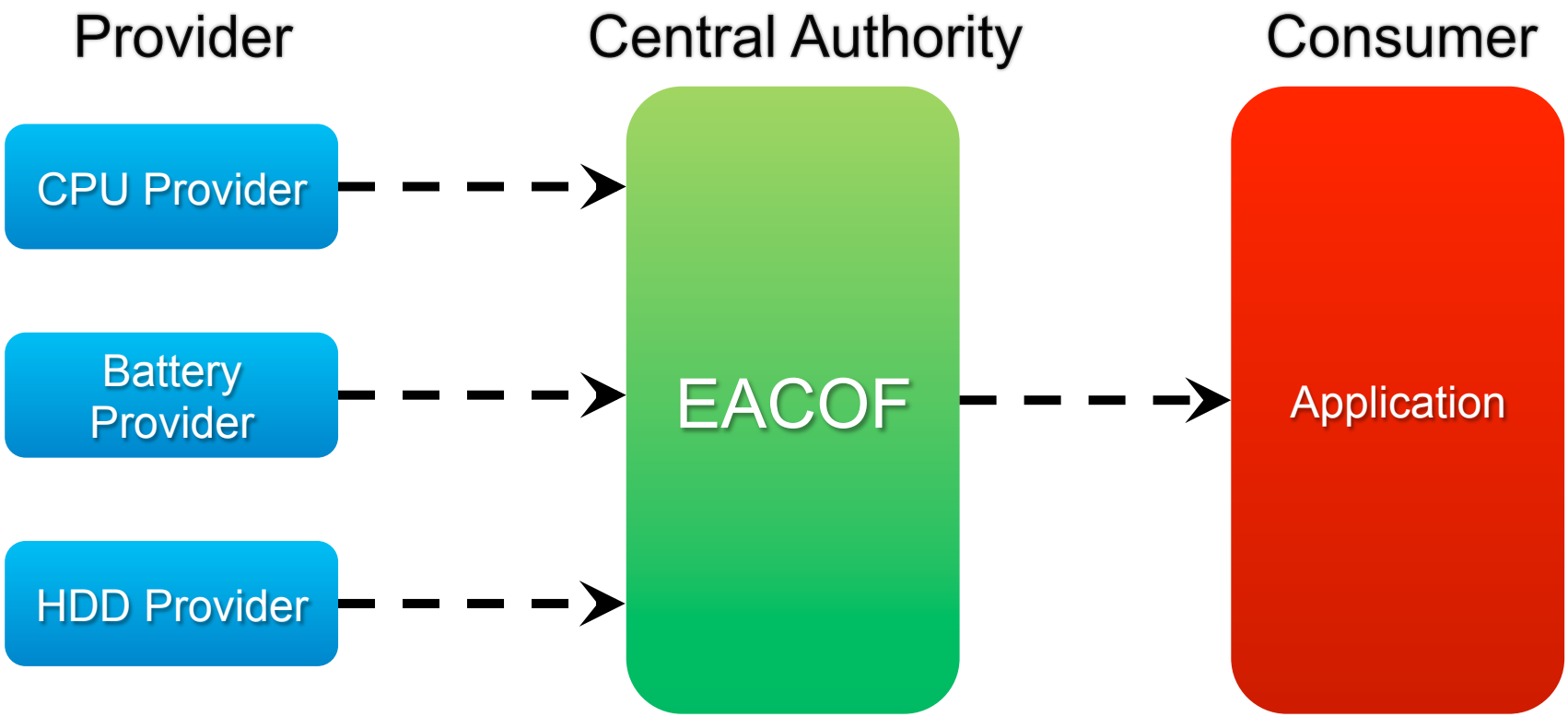
A simple Energy-Aware COmputing Framework

https://github.com/eacof

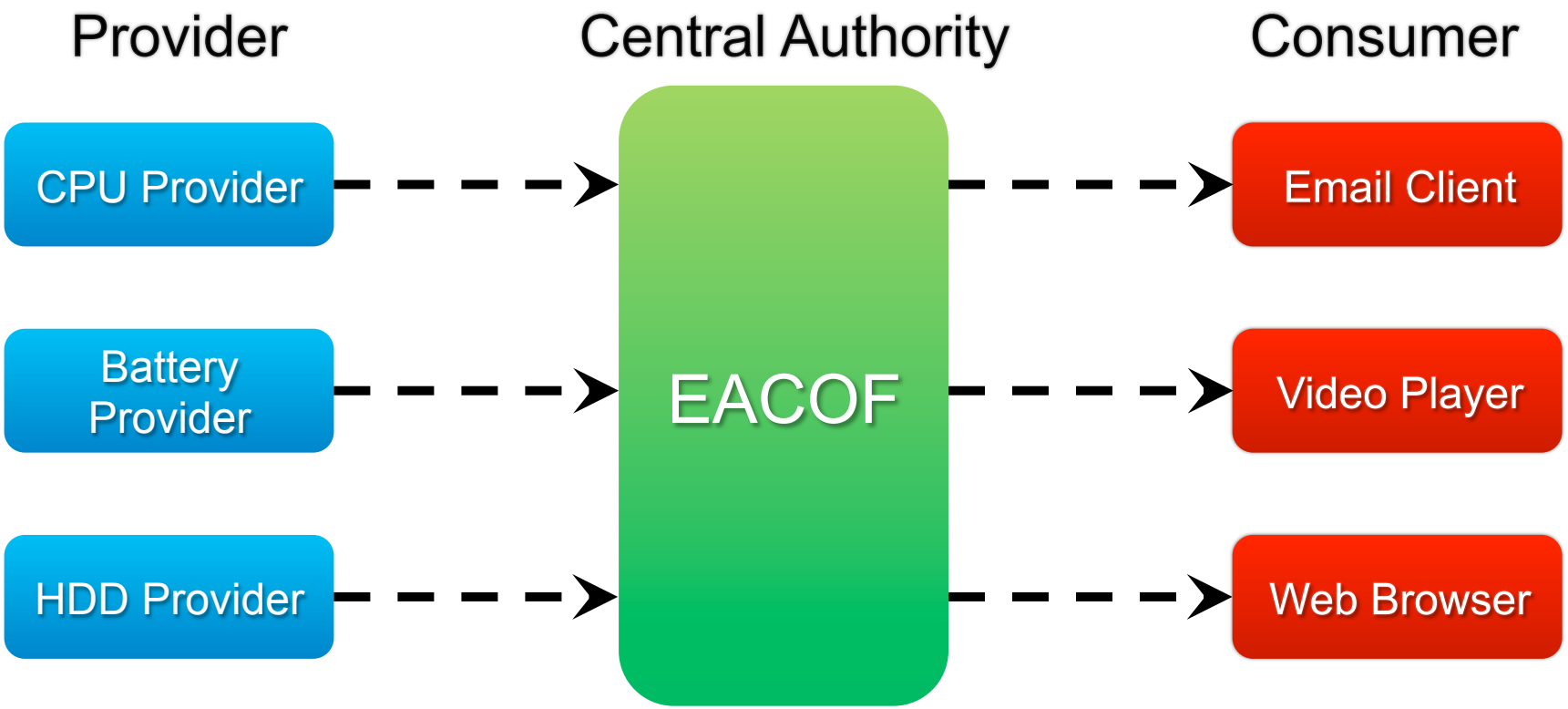
High Level


Provider
Central Authority
Consumer
Energy Data From Hardware or OS
EACOF
Application

Providers


Provider
Central Authority
Consumer
CPU Provider
Battery Provider
HDD Provider
EACOF
Application

Consumers


Provider
Central Authority
Consumer
CPU Provider
Battery Provider
HDD Provider
EACOF
Email Client
Video Player
Web Browser

Comparing Sorting Algorithms

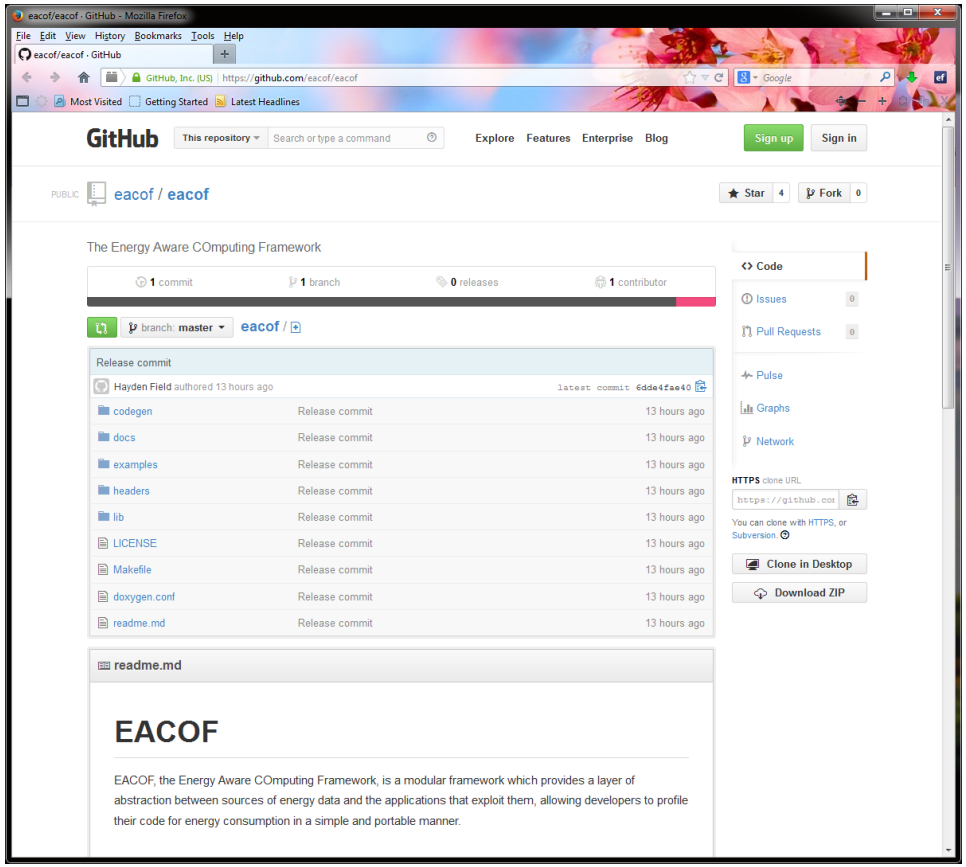
- Sorting of integers in [0,255]

		Data Type											
		uint8_t			uint16_t			uint32_t			uint64_t		
Algorithm	Num Elements	Total Time (s)	Total Energy (J)	Average Power (W)	Total Time (s)	Total Energy (J)	Average Power (W)	Total Time (s)	Total Energy (J)	Average Power (W)	Total Time (s)	Total Energy (J)	Average Power (W)
Bubble Sort	50,000	5.53	66.66	12.03	5.39	65.29	12.09	5.66	69.05	12.19	5.78	71.83	12.41
Insertion Sort	200,000	7.98	■102.18	12.75	7.98	■103.00	12.85	7.46	■98.81	13.21	7.54	■105.03	13.89
Quicksort	2,000,000	5.51	61.73	11.20	5.53	61.90	11.19	5.52	61.60	11.15	5.51	62.90	★11.42
Merge Sort	60,000,000	•6.06	•72.33	11.93	6.07	72.46	11.93	6.12	75.65	12.36	•5.93	•76.98	★12.98
qsort	100,000,000	•5.84	•72.39	12.37	6.15	76.90	12.48	6.79	86.29	12.69	•5.69	•73.25	12.86
Counting Sort	200,000,000	0.23	♦2.92	12.75	0.24	♦3.16	13.23	0.25	♦3.58	14.15	0.35	♦5.12	14.44

- ■ Insertion Sort: 32 bit version more optimized
- ♦ Counting Sort:
  75% more energy for 64 bit compared to 8 bit values
- • Sorting 64 bit values takes less time than sorting 8 bit values, but consumed more energy
- ★ Average power variations between algorithms

H. Field, G. Anderson and K. Eder. “EACOF: A Framework for Providing Energy Transparency to enable Energy-Aware Software Development”. *29th ACM Symposium On Applied Computing*. pp. 1194–1199. March 2014, ACM.

EACOF on github: Get involved!



github.com/eacof

Static Analysis for Energy Consumption

ENTRA

Whole-Systems
Energy Transparency

The ENTRA Project

- Whole Systems ENergy TRAnsparency

EC FP7 FET MINECC:

"Software models and programming methodologies supporting the strive for the energetic limit (e.g. energy cost awareness or exploiting the trade-off between energy and performance/precision)."

Static Energy Usage Analysis

Original Program:

```
int fact (int x) {
  if (x<=0)a
     return 1b;
  return (x *d fact(x-1))c;
}
```

Extracted Cost Relations:

$$C_{fact}(x) = C_a + C_b \quad \text{if } x<=0$$
$$C_{fact}(x) = C_a + C_c(x) \quad \text{if } x>0$$
$$C_c(x) = C_d + C_{fact}(x-1)$$

- Substitute C_a, C_b, C_d with
  the **actual energy required to execute the corresponding lower-level (machine) instructions.**

Energy Modelling

Energy Modelling

Energy Cost *(E)* of a program *(P)*:

$$E_P = \sum_i (B_i \times N_i) + \sum_{i,j} (O_{i,j} \times N_{i,j}) + \sum_k E_k$$

Instruction Base Cost, B_i, of each instruction i

Circuit State Overhead, $O_{i,j}$, for each instruction pair

Other Instruction Effects (stalls, cache misses, etc)

V. Tiwari, S. Malik and A. Wolfe. “Instruction Level Power Analysis and Optimization of Software”, Journal of VLSI Signal Processing Systems, 13, pp 223-238, 1996.

XCore Energy Modelling

Energy Cost *(E)* of a multi-threaded program *(P)*:

$$E_{\mathrm{p}} = P_{\mathrm{base}} N_{\mathrm{idle}} T_{\mathrm{clk}} + \sum_{t=1}^{N_t} \sum_{i \in \mathrm{ISA}} \left(\left(M_t P_i O + P_{\mathrm{base}} \right) N_{i,t} T_{\mathrm{clk}} \right)$$

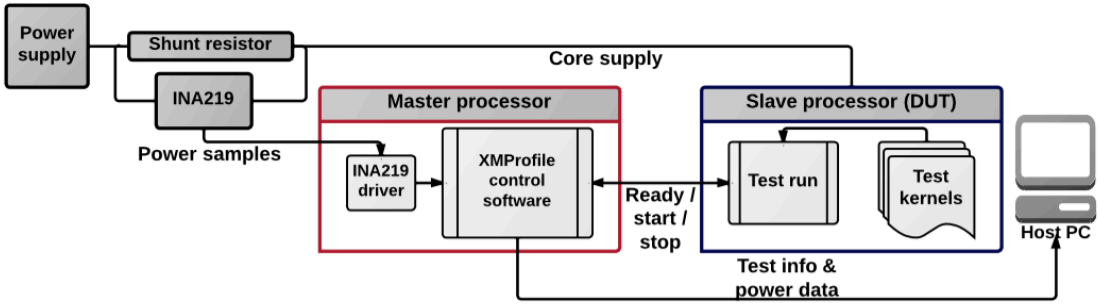
Idle base power and duration

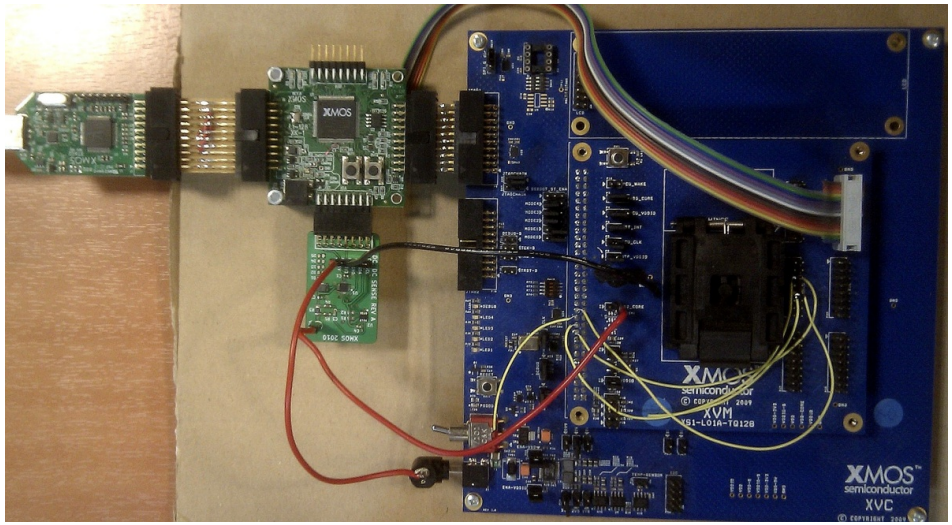
Concurrency cost, instruction cost, generalised overhead, base power and duration

- Use of execution statistics rather than execution trace.
- Fast running model with an average error margin of less than 7%

S. Kerrison and K. Eder, 2015. “Energy Modelling of Software for a Hardware Multi-threaded Embedded Microprocessor”, ACM Transactions on Embedded Computing Systems (TECS). To appear.

The set up...





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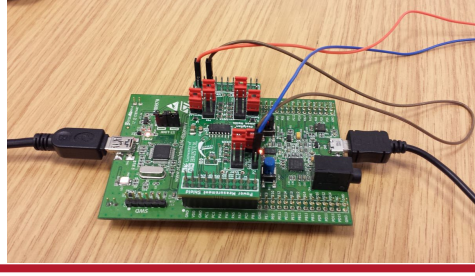
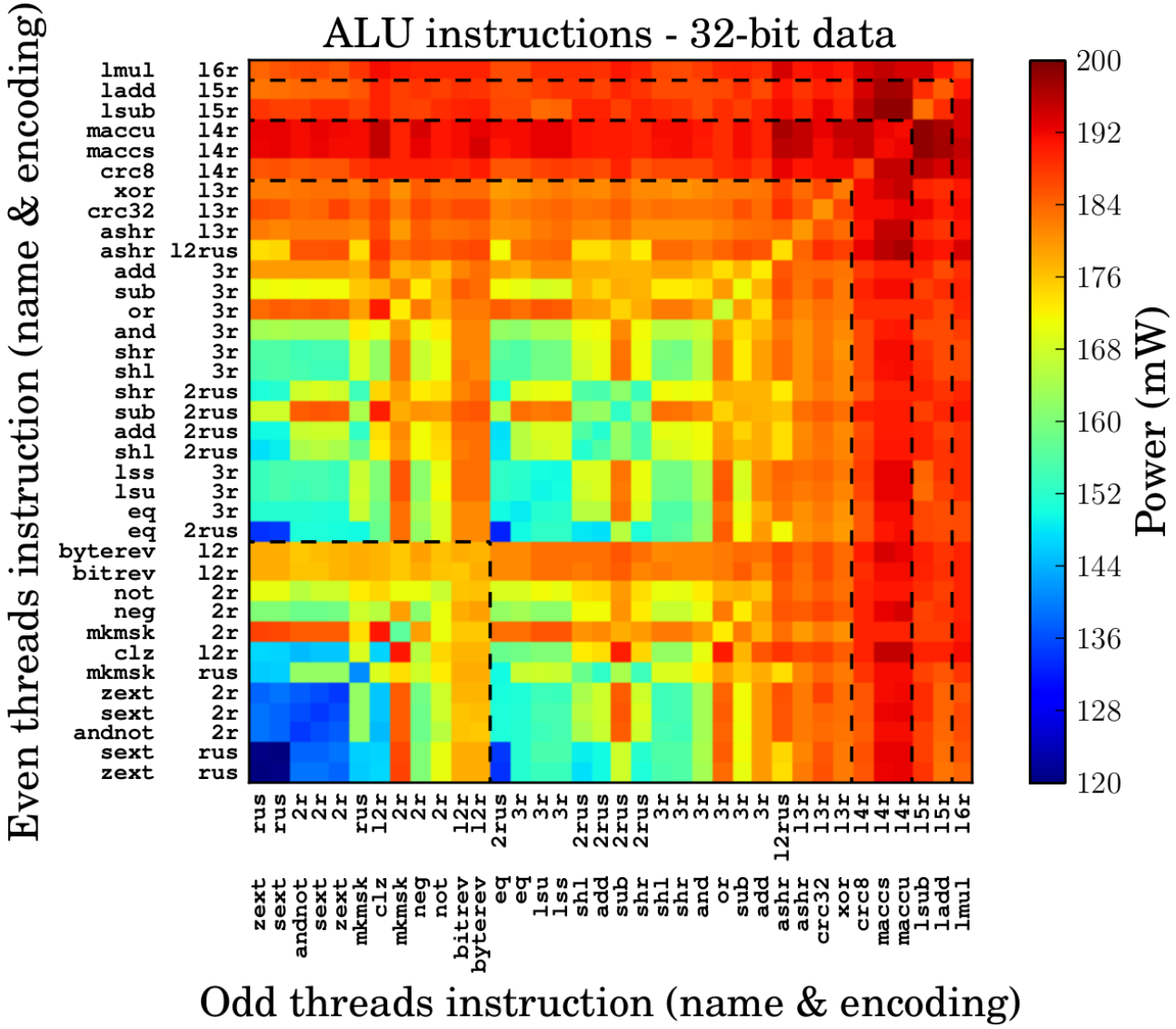
ISA Characterization





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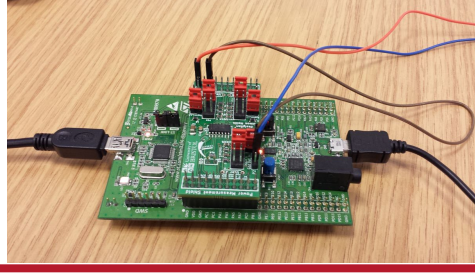

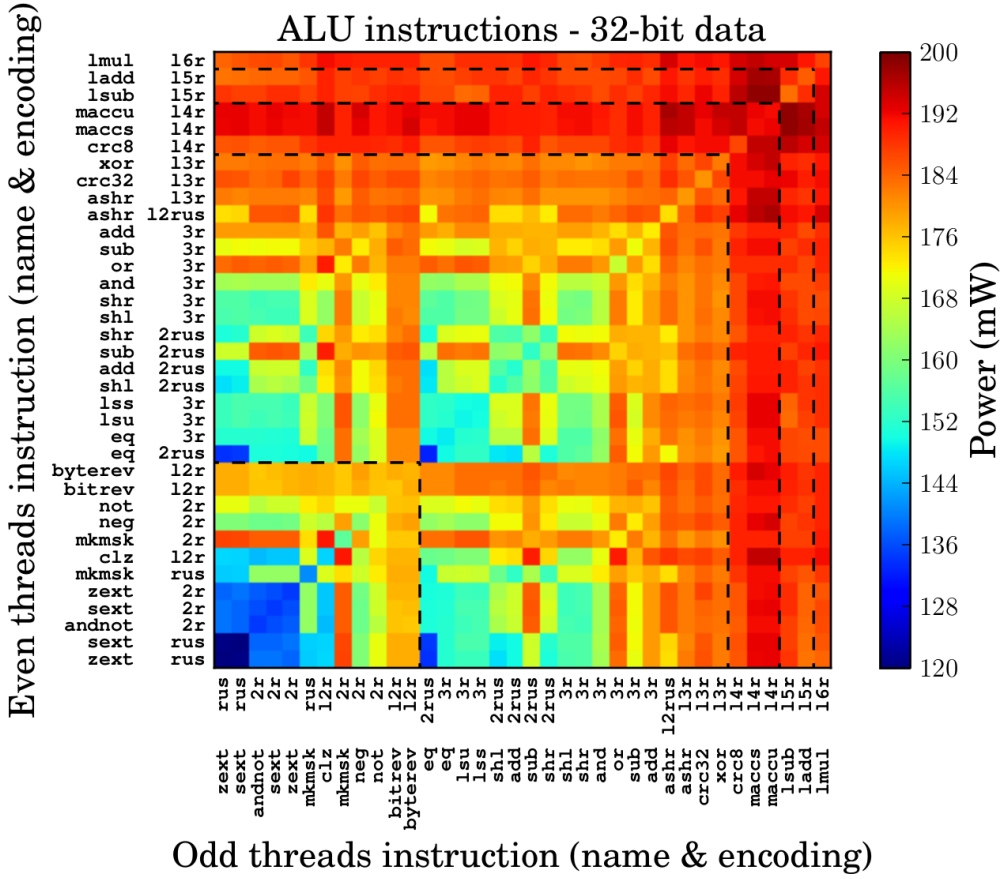

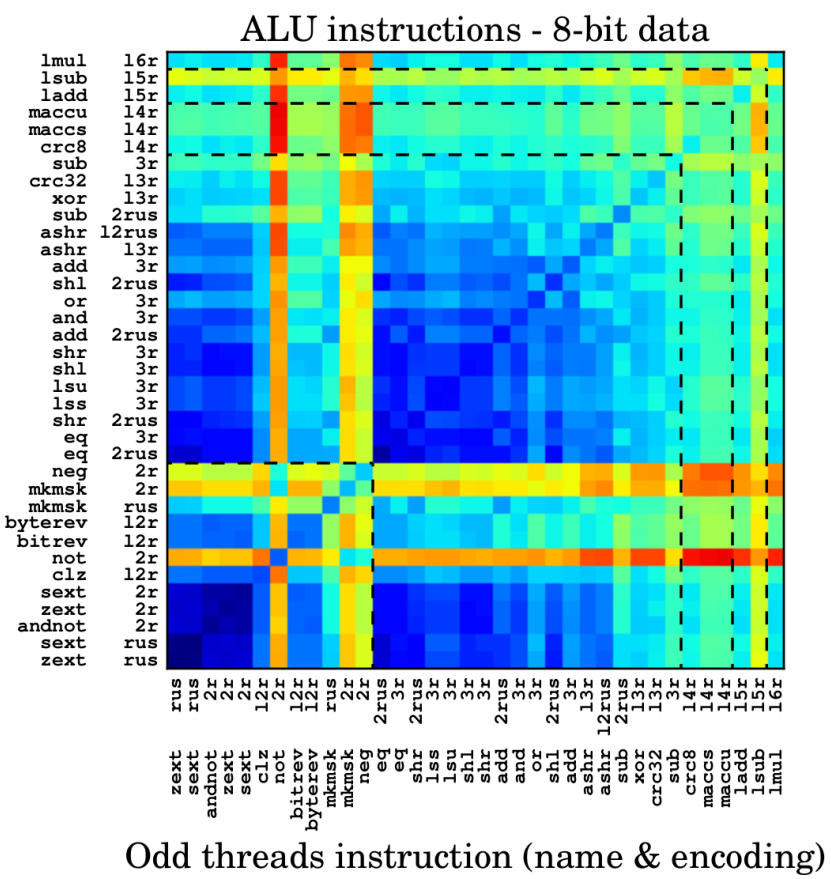

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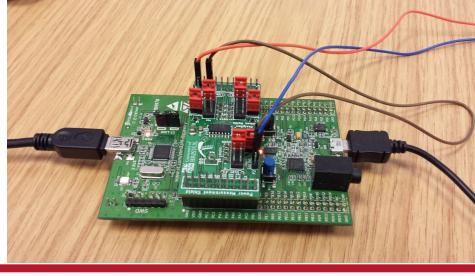
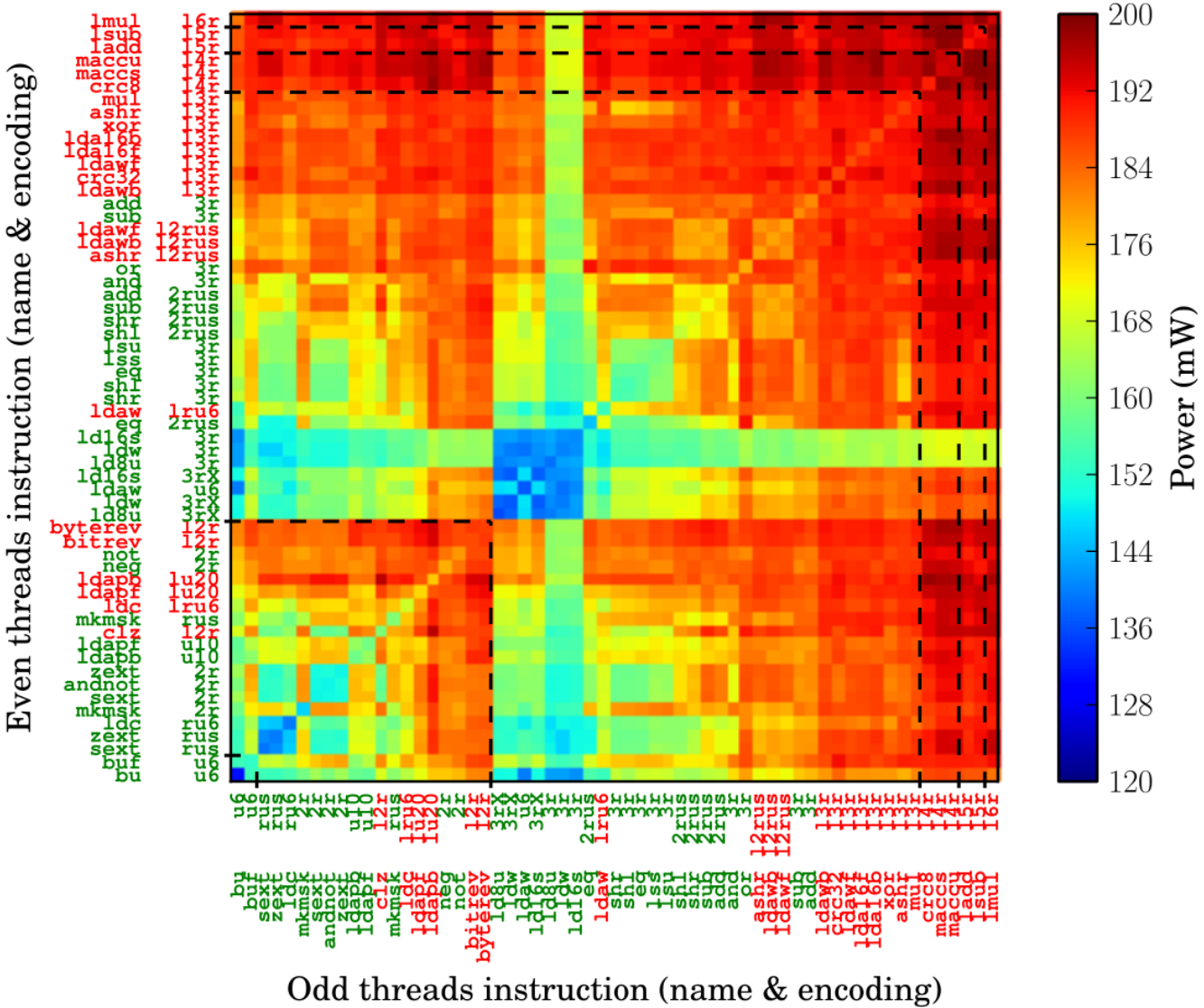
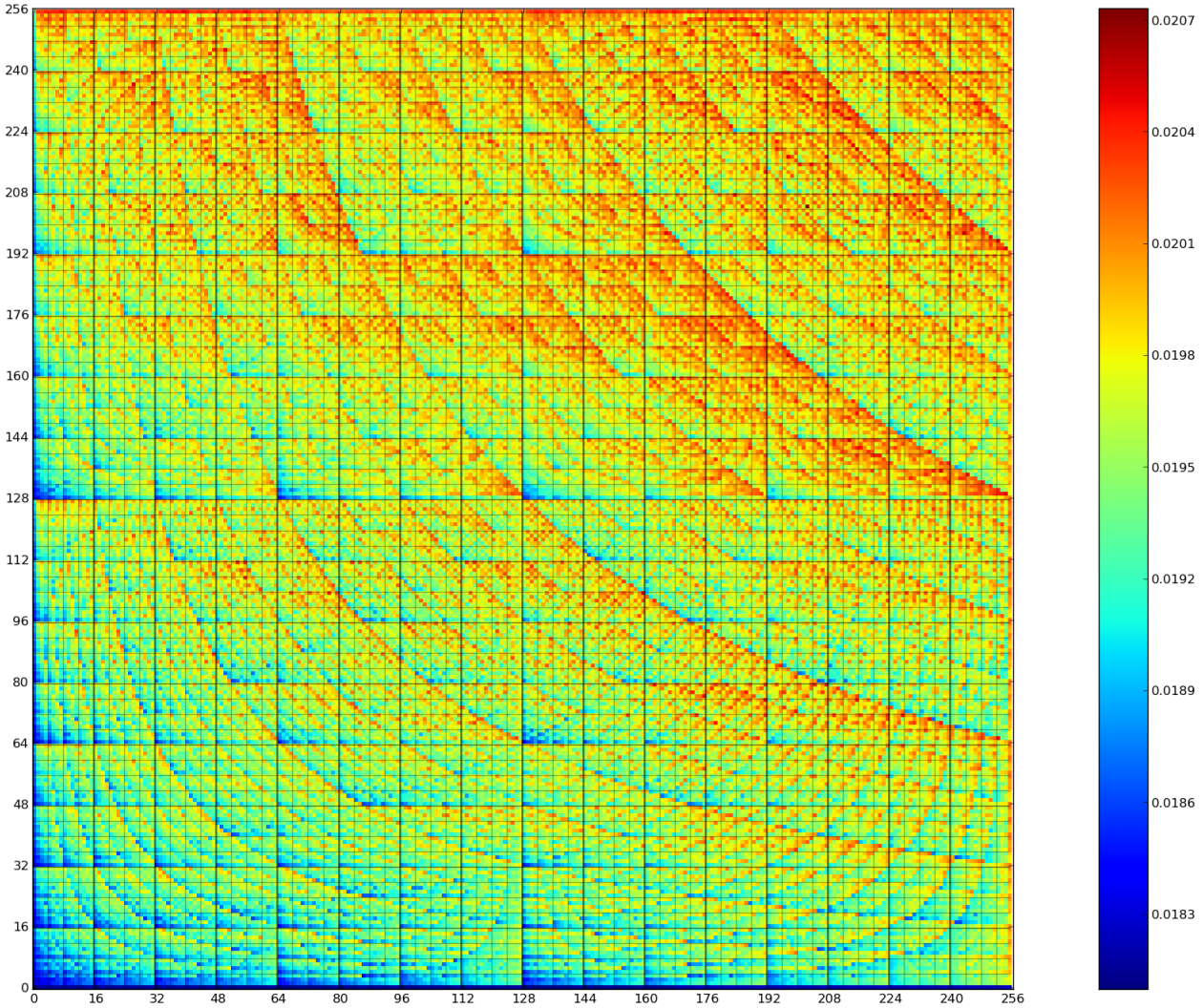




ISA Characterization Insights

Is a*b = b*a?

Is a*b = b*a?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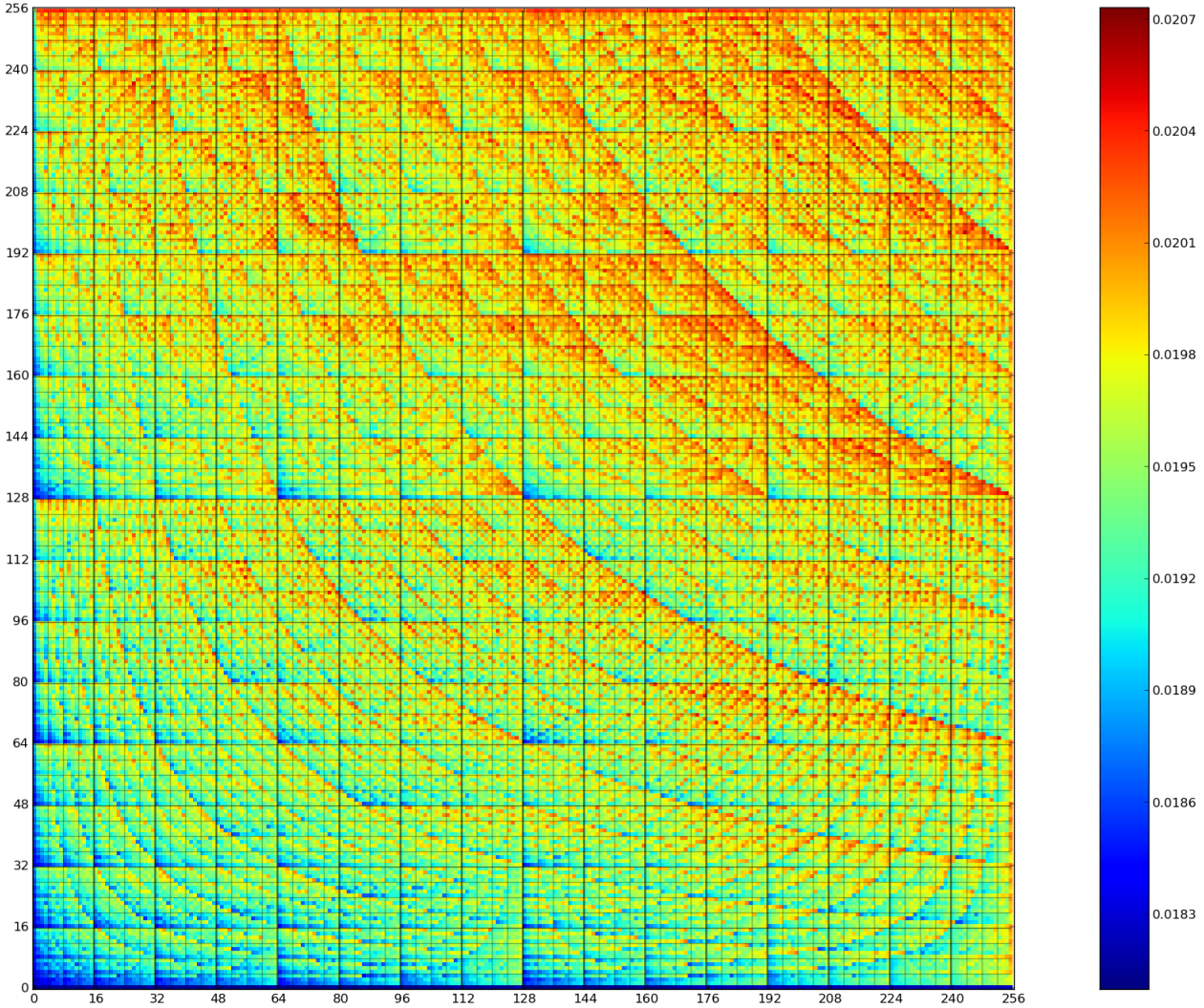
E(a*b) ≠ E(b*a)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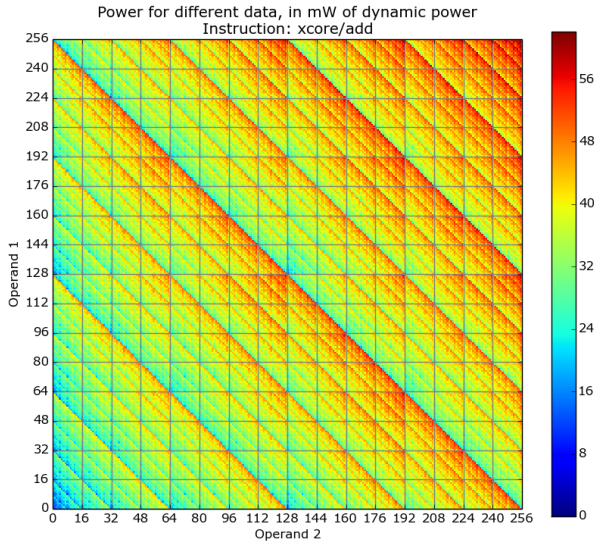
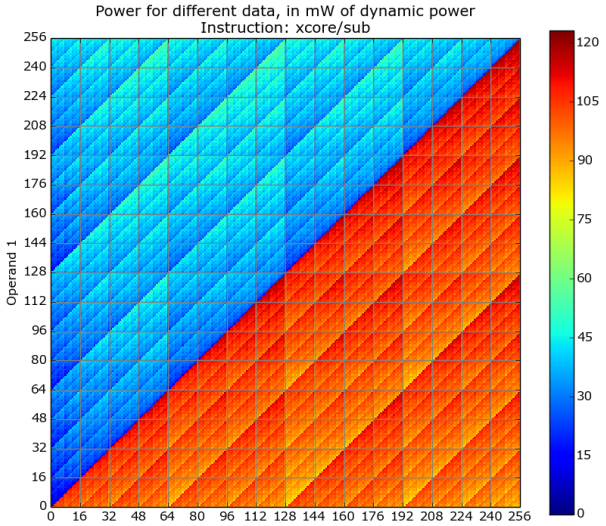
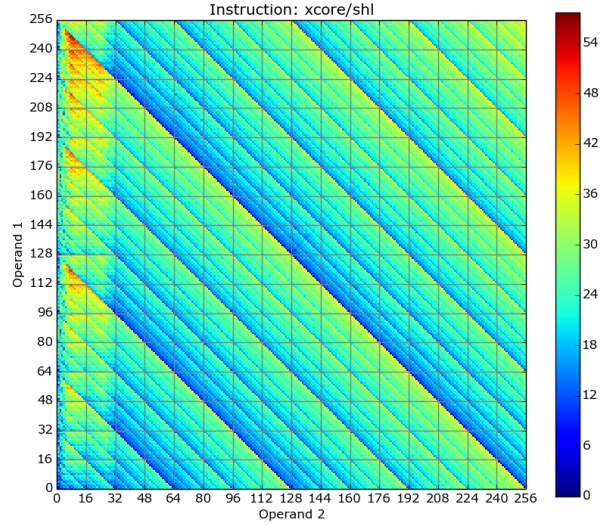
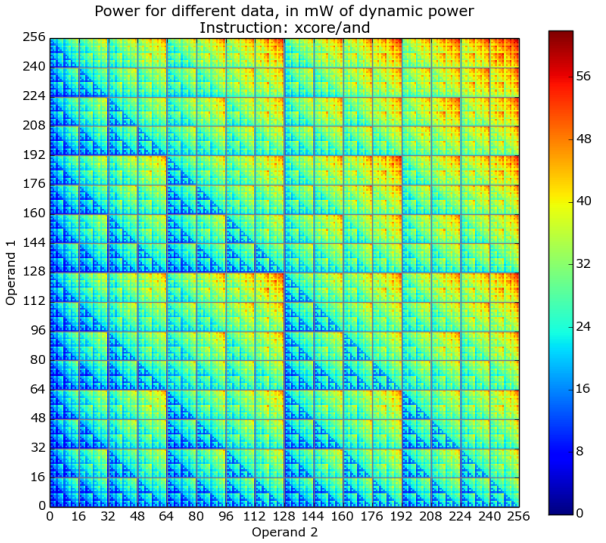
W/A/B-Case Energy Consumption





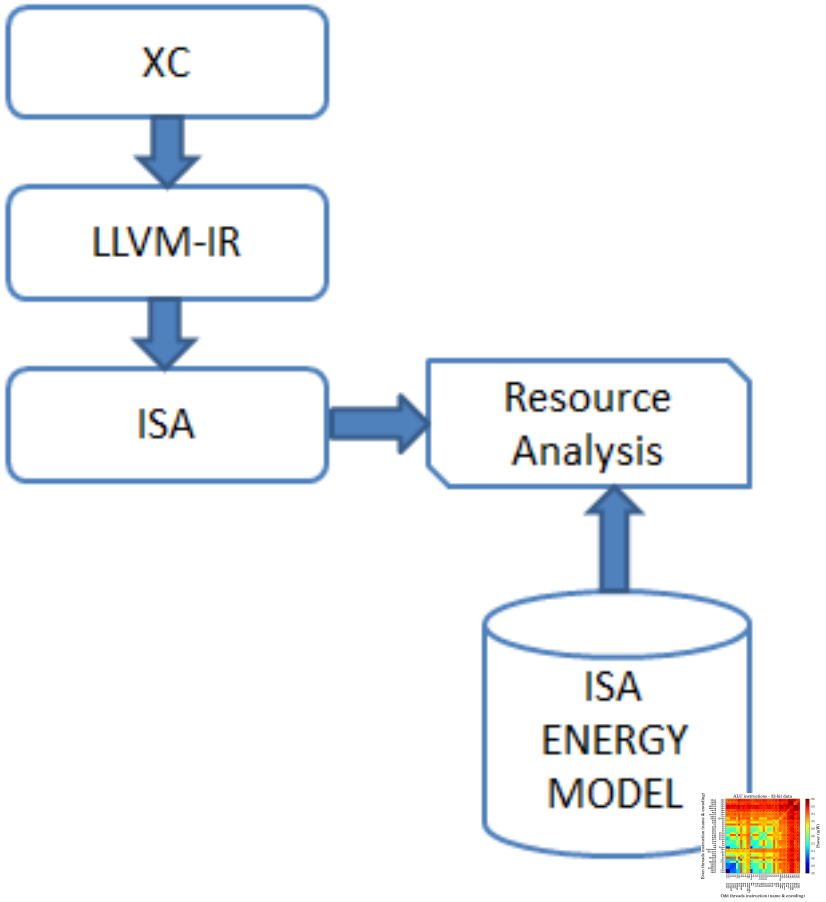




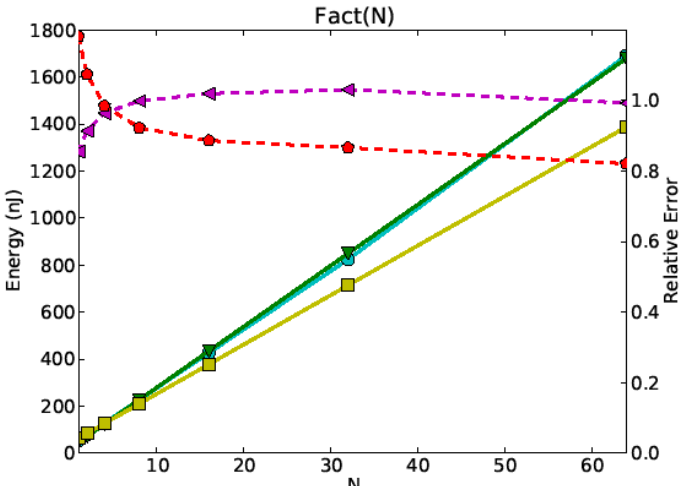
Energy Consumption Analysis

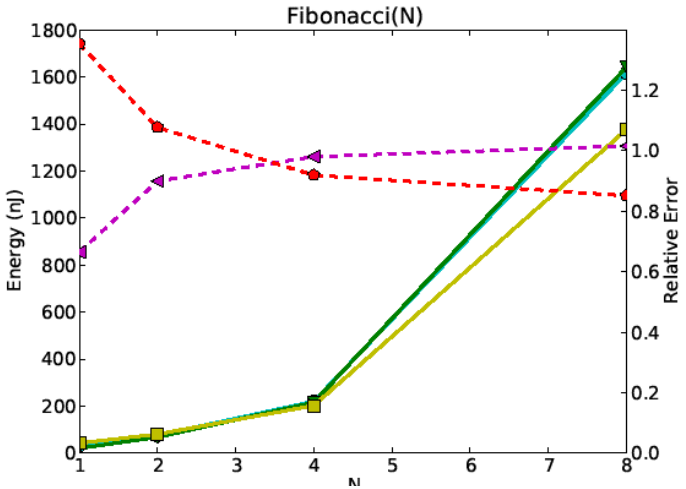
Analysis at the ISA Level

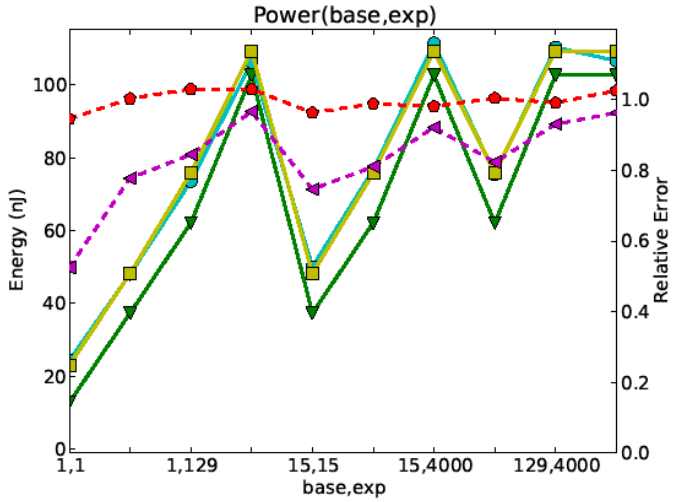
- Combine static resource analysis (SRA) with the ISA-level energy model.
- Provide energy consumption function parameterised by some property of the program *or its data*.

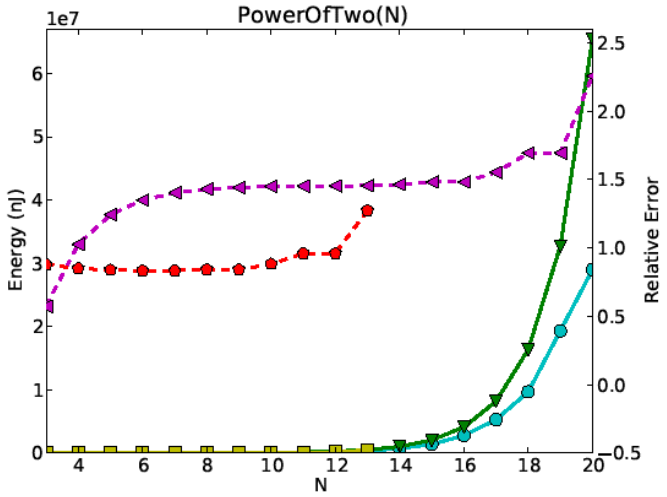


ISA-Level Analysis Results



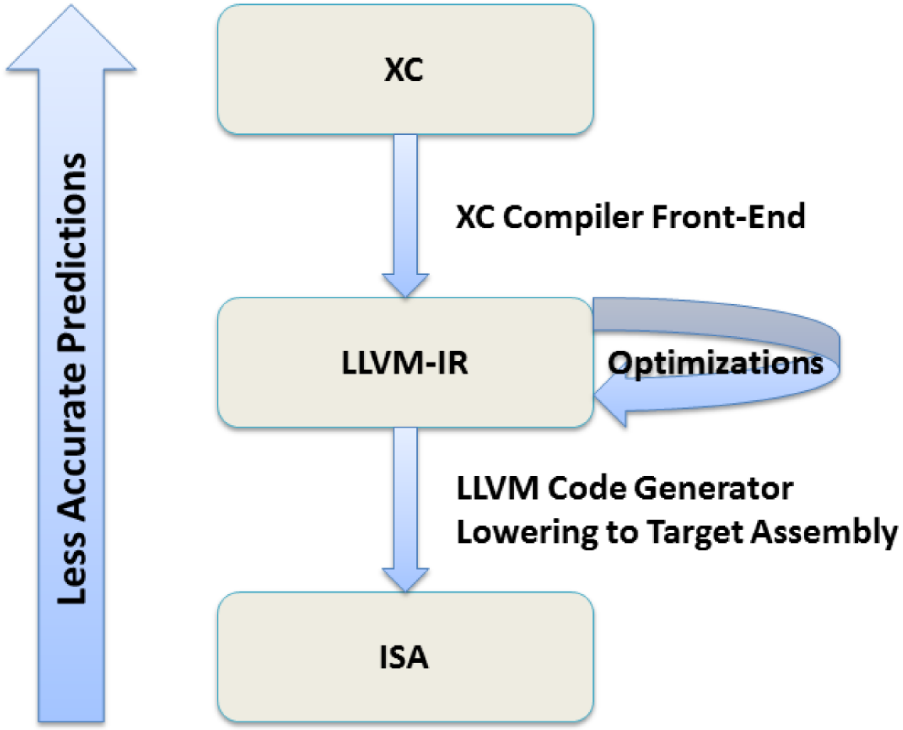






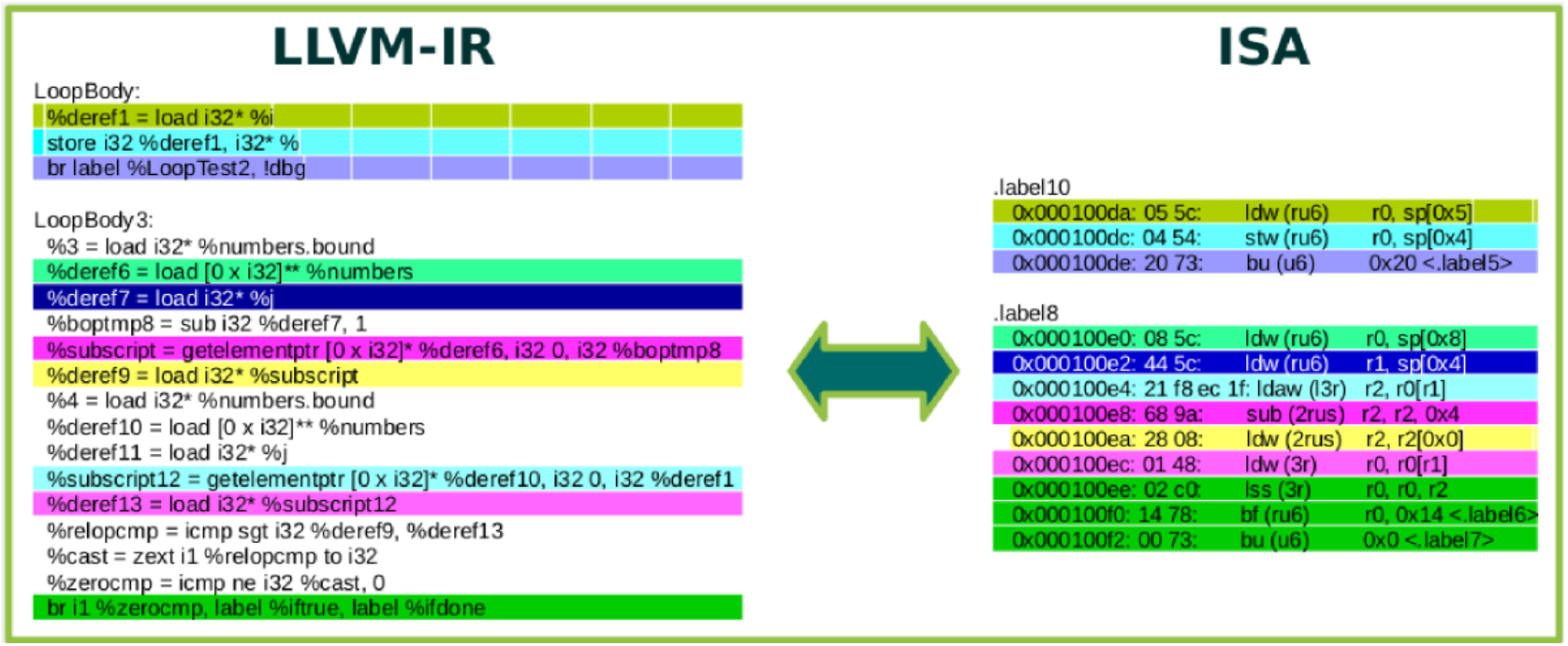
U. Liqat, S. Kerrison, A. Serrano, K. Georgiou, N. Grech, P. Lopez-Garcia, M.V. Hermenegildo and K. Eder. "Energy Consumption Analysis of Programs based on XMOS ISA-Level Models". LOPSTR 2013.

Analysis Options



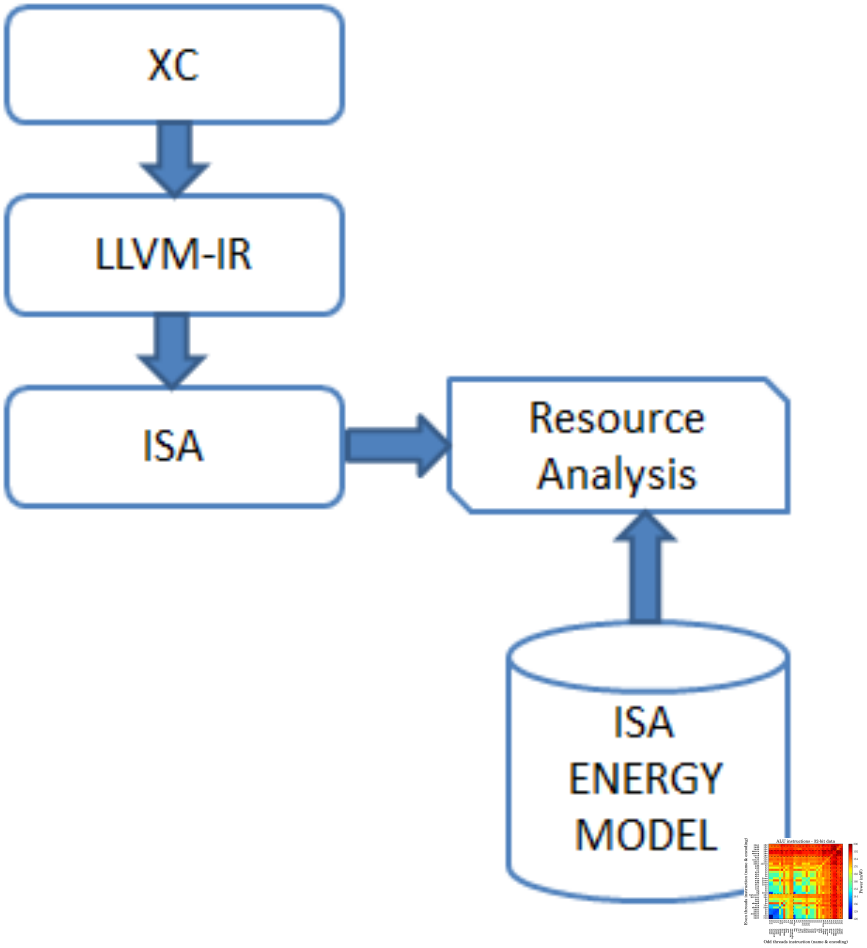
- Moving away from the underlying model risks loss of accuracy.
- But it brings us closer to the original source code.

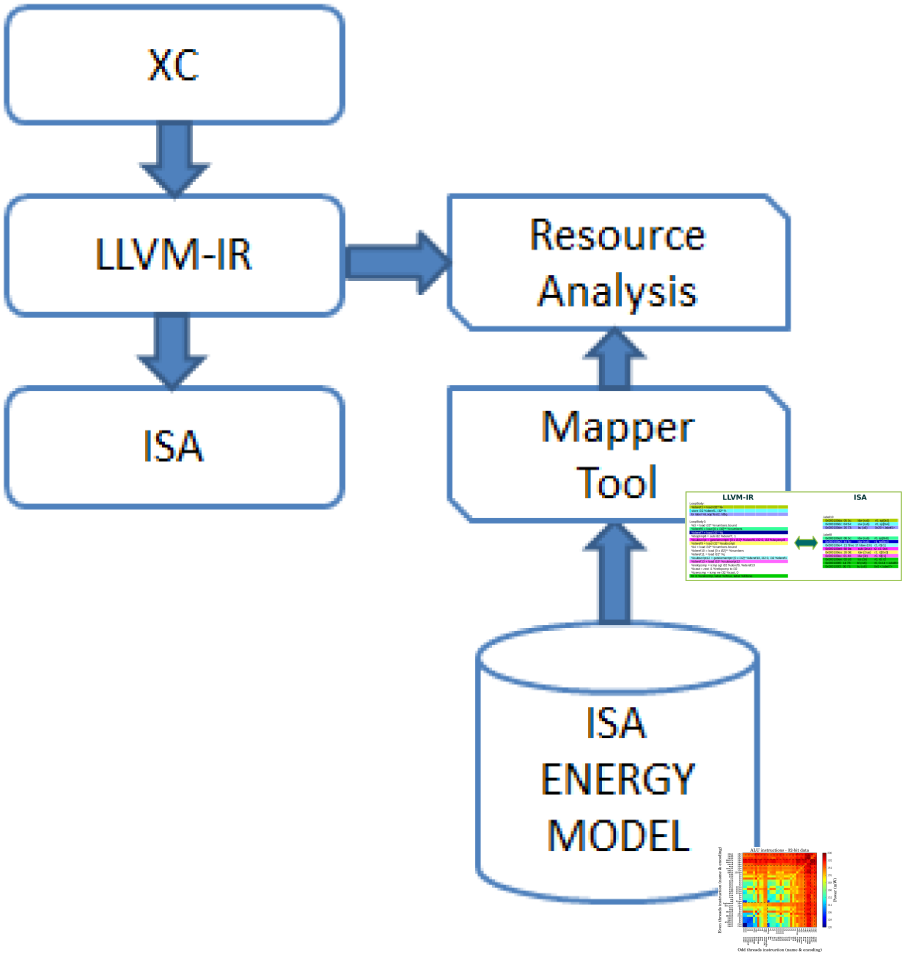
Mapping LLVM IR to Assembly



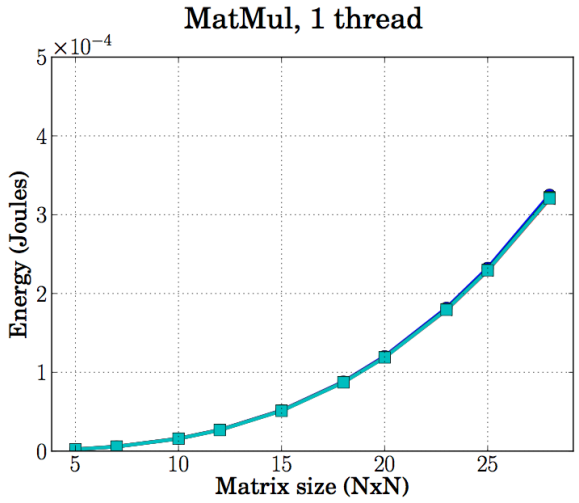
K. Georgiou, S. Kerrison and K. Eder, 2015. “A Multi-level Worst Case Energy Consumption Static Analysis for Single and Multi-threaded Embedded Programs”, ACM Transactions on Architecture and Code Optimization (TACO). To be submitted; draft available on request.

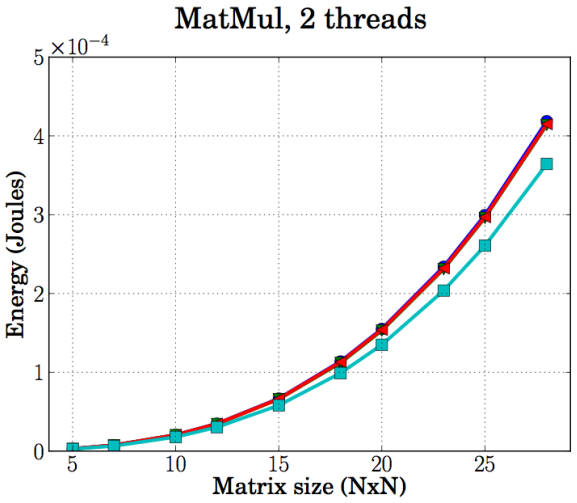
Analysis at the LLVM-IR Level

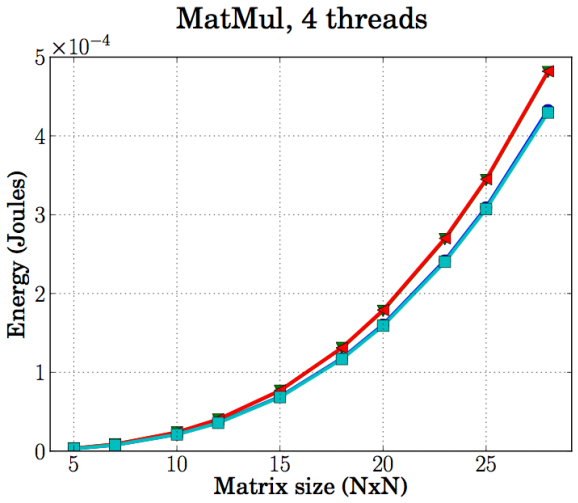


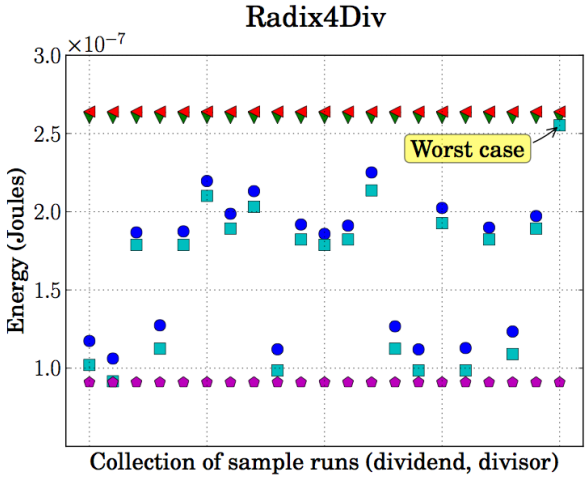


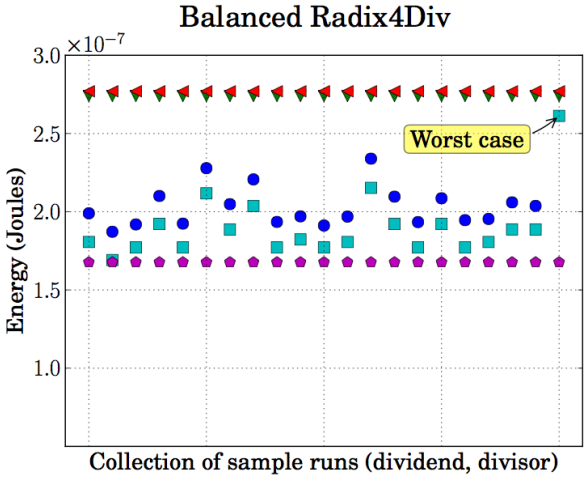
WCEC Static Analysis Results

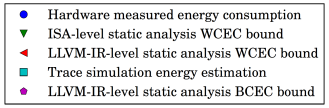












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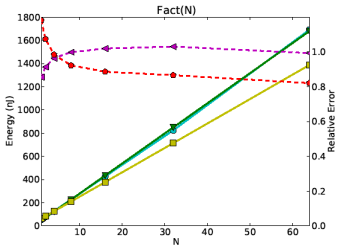
Towards Energy Aware Software Engineering

Energy Transparency



- For HW designers:
  "Power is a 1st and last order design constraint."

  [Dan Hutcheson, VLSI Research, Inc., E^{3}S Keynote 2011]

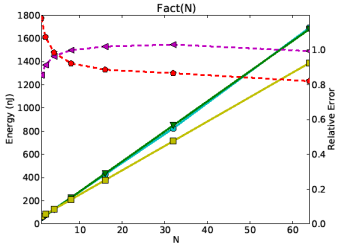
- "Every design is a point in a 2D plane."

  [Mark Horowitz,E^{3}S 2009]

Scaling Power and the Future of CMOS

Mark Horowitz, EE/CS Stanford University

Energy Transparency



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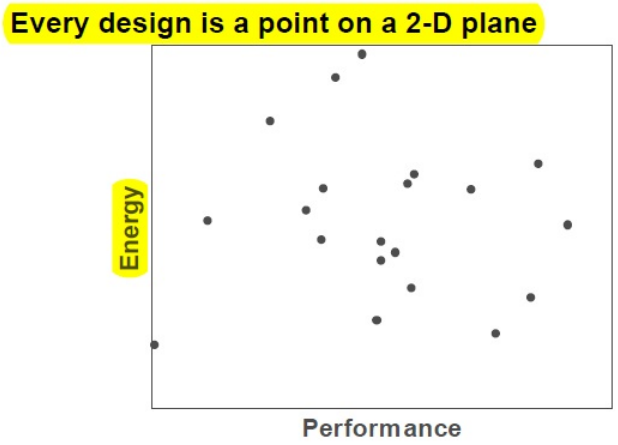
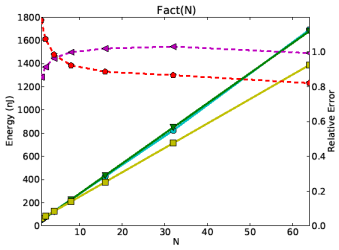
Optimizing Energy



Energy Transparency



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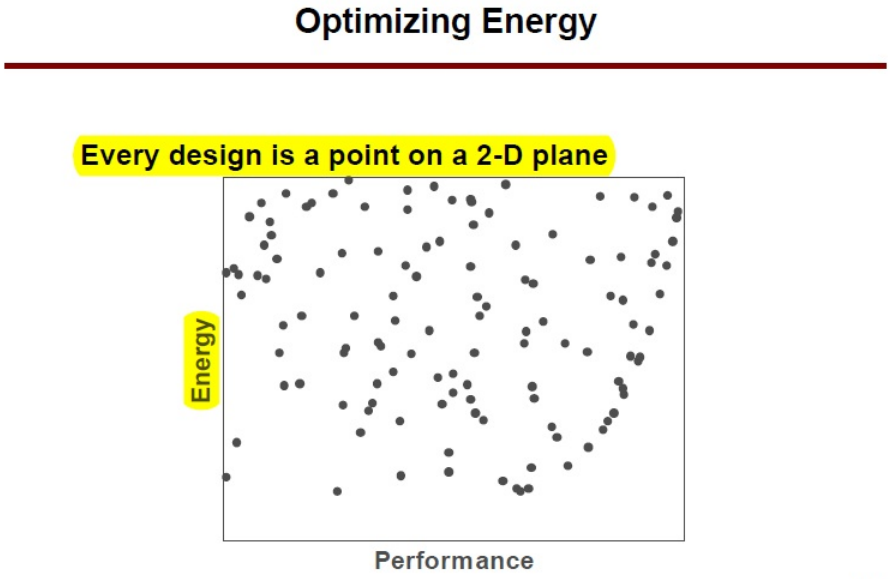

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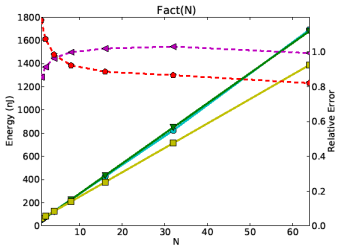

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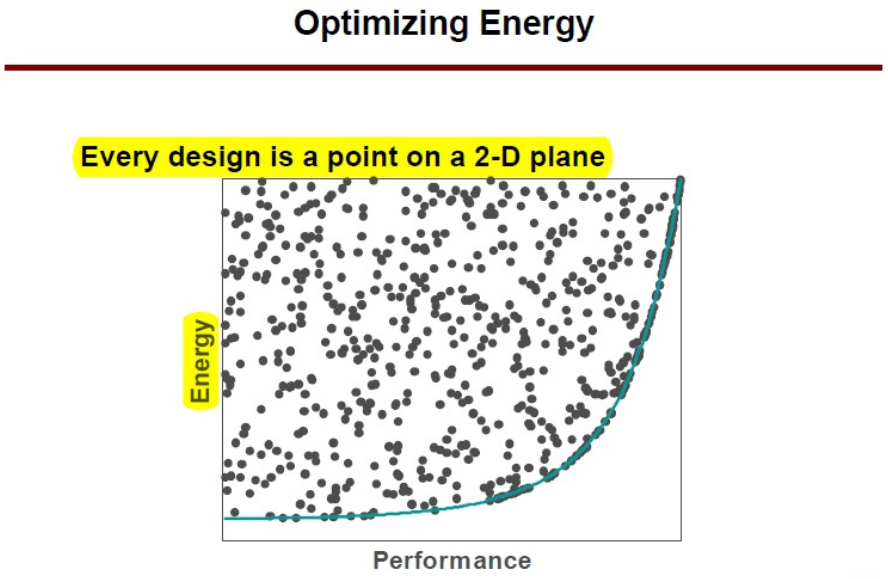
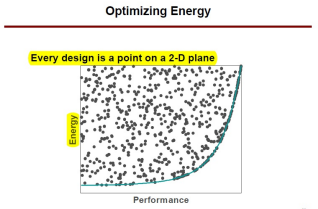


More POWER to SW Engineers

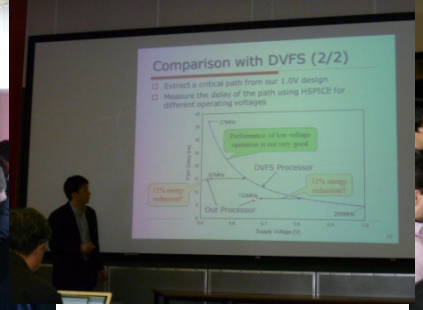


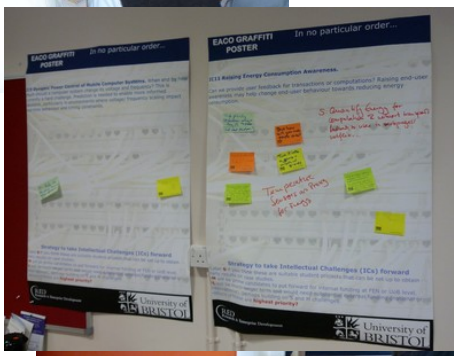

```
in 5pJ do {...}
```

- Full **Energy Transparency** from HW to SW
- Location-centric programming model

- **“Cool” code**
  A cool programming competition!

Promoting energy efficiency to a 1st class SW design goal is an urgent research challenge.

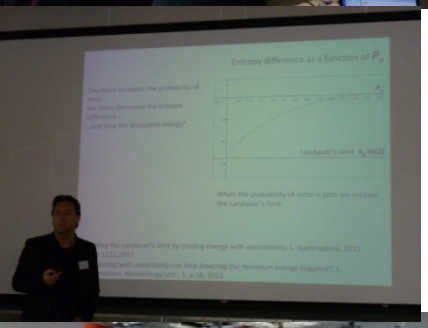




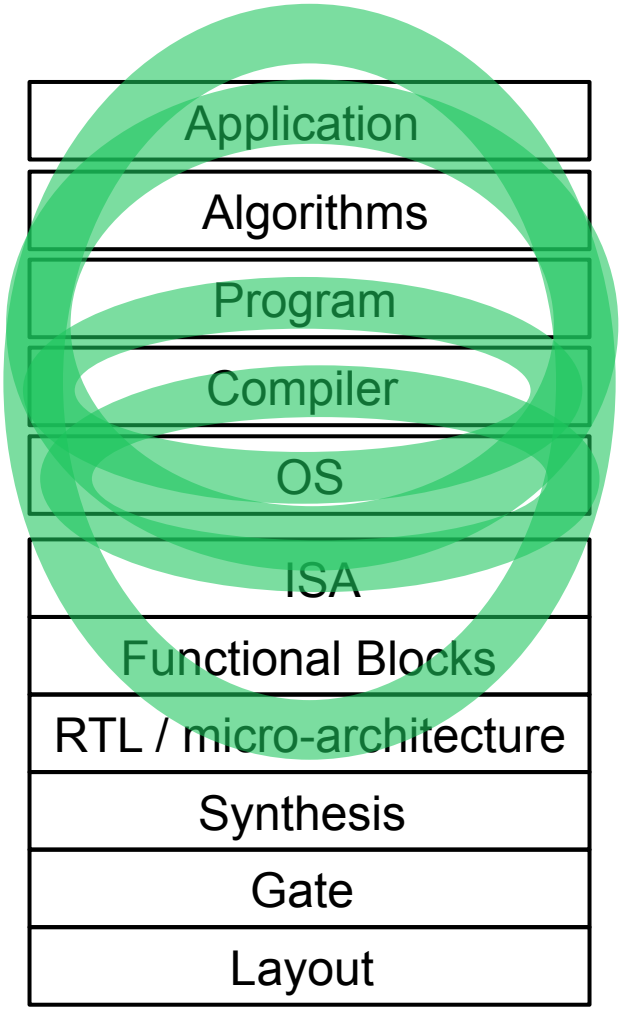
EACO @ Bristol

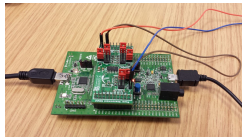
The Energy-Aware COmputing Initiative, Research Agenda and Workshops

http://www.cs.bris.ac.uk/Research/Micro/eaco.jsp

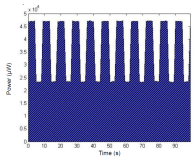


EACO Research at Bristol

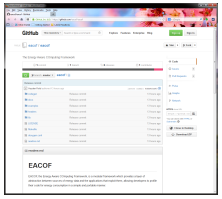




- EACO Platform
  - Online power monitoring
  - RTOS API

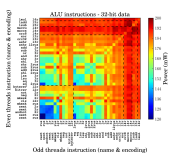


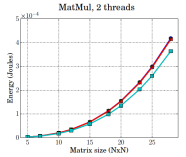
- EACOF (github.com/eacof)
  - API for SW energy measurement



- Machine Guided Energy Efficient Compilation (MAGEEC)

- Superoptimization for low energy
- Whole Systems Energy Transparency (ENTRA)





ICTenergy

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ICTenergy

Welcome to the ICT-Energy project website!

The goal of the project is to create a coordination activity among consortia involved in the ICT-Energy field with specific reference to bringing together the existing "Toward Zero-Power ICT" community organized within the ZEROPOWER project and the novel "MINECC" (Minimising energy consumption of computing to the limit) community recently funded under the FET Proactive Call 8 (FP7-ICT-2011-8) Objective 9.8. The coordination activity is aimed at assessing the impact of the research efforts developed in the groups involved in the different consortia and proposing measures to increase the visibility of ICT-Energy related initiatives to the scientific community, targeted industries and to the public at large through exchange of information, dedicated networking events and media campaigns.

Please visit the website to stay informed on our news and initiatives. We hope you find the information in this website interesting and stimulating. If you want to know more about the project or its topic, please do not hesitate to contact us.

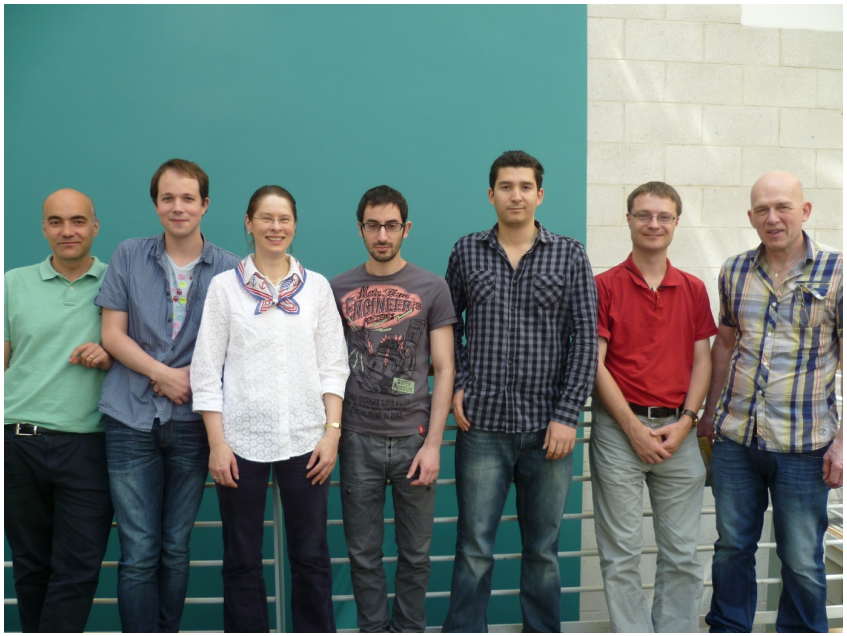
ICT-ENERGY

NANOENERGY LETTERS

NANOENERGY Letters becomes ICT-ENERGY Letters. The change in name reflects our intention to keep our promise to become the scientific journal of a rapidly growing community interested in the various aspects associated with the role of energy in Information and Communication Technology. In this issue, as it is customary, we present some news together with scientific articles and documents. On the news side we report on the conclusion of the EC funded 3-year coordination action (c.a.) denominated ZEROPOWER. In the meantime, the novel c.a. ICT-Energy (see www.ict-energy.eu) has taken over the role of promoting the activities in this field and we acknowledge the emergence of this novel community by welcoming in our editorial board representatives from the various consortia involved in the c.a. ICT-Energy. It is worth mentioning that in this issue we publish the updated version of the ZEROPOWER Strategic Research Agenda. This is an important document that has the ambition to help defining the state of the art of the research in this field and to draw the lines for future developments. Finally I would like to mention the recent publication of the new science book entitled *ICT-Energy. Concepts Towards Zero - Power Information and Communication Technology.* This is freely available for download at the INTECH web site: http://www.intechopen.com/books. (LG)

http://www.ict-energy.eu/

Thank you for your attention



Kerstin.Eder@bristol.ac.uk