

# Software-based Fault Tolerance – Mission (Im)possible?

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The 29th CREST Open Workshop on Software Redundancy November 18, 2013







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#### Soft-Errors (Transient hardware faults)

- Induced by e.g., radiation, glitches, insufficient signal integrity
- Affecting microcontroller logic



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  - Affecting microcontroller logic
- Future hardware designs: more performance and parallelism
  → On the price of being less and less reliable



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### Software-Based Fault Tolerance



#### Software-based redundancy

- Triple Modular Redundancy (e.g., recommended by ISO 26262)
- Selective and adaptive
- ✓ Resource efficient



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#### Software-based redundancy

- Triple Modular Redundancy (e.g., recommended by ISO 26262)
- Selective and adaptive
- ✓ Resource efficient
- Single points of failure
  - Interface and Majority Voter
  - Allowing for Silent Data Corruptions (SDC)
  - → Replication is impossible!



### Threats to Applicability – Mission failed?



Triple modular redundancy reliability

$$R_{TMR} = R_{Voter} \cdot R_{2-of-3}$$



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- Voting on unreliable hardware?
  - Very small → residual error probability?
  - Risk analysis  $\rightarrow$  inherently complex (no random error distribution! [4])



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  - Risk analysis → inherently complex (no random error distribution! [4])

### $\rightarrow$ Dealbreaker for software-based TMR









Eliminate single points of failure





- Eliminate single points of failure
- Constrain residual error probability





- Eliminate single points of failure
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- Dependability as a resource efficient option



# Agenda

Introduction

### The Combined Redundancy approach (CoRed)

- Holistic protection eliminating single points of failure
- Arithmetic coding
- Dependable voting

#### Constraining residual error probability

- From coding theory to application lessons learned
- Finding appropriate parameters
- Circumvent implementation pitfalls

#### Evaluation

- Use case
- Experimental setup
- Fault-injection results

### Conclusion





The <u>Combined Red</u>undancy Approach (*CoRed*) TMR +  $\begin{cases} \\ \\ \end{cases}$ 



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The <u>Combined Red</u>undancy Approach (CoRed)

TMR + Data-flow encoding<br/>Dependable voters



The <u>Combined Red</u>undancy Approach (CoRed)

TMR + Data-flow encoding<br/>Dependable voters

- Holistic protection approach for control applications
  - Input to output protection
    - 1 Reading inputs  $\rightarrow$  2 Processing  $\rightarrow$  3 Distributing outputs

# Eliminating Input and Output Vulnerabilities



#### Arithmetic Codes → ANBD Code

- Based on VCP [5]
- Data integrity:
- Address integrity:
- Outdated data:

Key

Per variable signature Timestamp  $v' = A \cdot v + B + D$ 



# Eliminating Input and Output Vulnerabilities



#### ■ Arithmetic Codes → ANBD Code

- Based on VCP [5]
- **Data integrity:** Key
- Address integrity: Per variable signature
- Outdated data: Timestamp

 $v' = A \cdot v + B + D$ 

- Set of arithmetic operators (+, -, \*, =, ...)
  - Checksum vs. Arithmetic code (AN code)
  - AN Code → Encoded data operations
  - Enabler for dependable voter



### CoRed Dependable Voter – Basics



#### CoRed Dependable Voter

- Input: variants (X', Y', Z')
- Output: Equality set (E) and encoded winner (W)
- No decoding necessary

#### Control-flow signatures

- Static signature (expected value): Compile-time
  - $\rightarrow$  Used as return value E
- Dynamic signature (actual value): Runtime, computed from variants  $\rightarrow$  Applied to winner W
- Validation: Subsequent check (decode)



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### From Coding Theory to Application





### Constraining residual error probability



#### Coding theory

- Data word + redundant information = code word
- Fault detection → distance between code words

$$v' = A \cdot v + B + D$$

### Constraining residual error probability



#### Coding theory

- Data word + redundant information = code word
- Fault detection → distance between code words
- Residual error probability
  - Chance for code-to-code word mutation
  - Fundamental property for fault tolerance mathematics

$$v' = A \cdot v + B + D$$

$$p_{sdc} = \frac{\text{valid code words}}{\text{possible code words}} \approx \frac{1}{A}$$

### Constraining residual error probability



#### Coding theory

- Data word + redundant information = code word
- Fault detection → distance between code words
- Residual error probability
  - Chance for code-to-code word mutation
  - Fundamental property for fault tolerance mathematics



### Choosing Keys and Signatures

### Mathematics: prime numbers

- Intuitively plausible
- Literature: little help to find suitable As

### Practitioner's approach: min. Hamming distance

- Distance (d) between code words (# unequal bits)
- *d-1* bit error detection capabilities

### Brute force

1.4×10<sup>14</sup> experiments for all 16 bit As

58 831	u <sub>min</sub> – 2	
<b>58,659</b>	6	5

### $\rightarrow$ The bigger the better is misleading!



1

1

0

1

1

0

0

0

### Consistence with Coding Theory – Mission Failed?



#### Fault-simulation → entire fault-space

- Each and every A, v and fault pattern
- $6.5 \times 10^{16}$  experiments for 16 bit As and 1-8 bit soft errors
- → Excess of predicted residual error probability
- $\rightarrow$  Violation of predicted fault-detection capabilities

![](_page_28_Picture_7.jpeg)

# Think Binary

![](_page_29_Figure_1.jpeg)

3×10<sup>-3</sup>

#### Binary representation of code words

- Coding theory is unaware of machine word sizes
- → Dangerous over- and underflow conditions
- Extended AN code (EAN) implementation
- → Compliance with coding theory!
- Improved code reliability (A = 251)
  - Predicted
  - Common implementation [4]  $\approx 1.3 \times 10^{-2}$
  - EAN implementation  $\approx 1.5 \times 10^{-5}$

#### → Improvement by orders of magnitude!

# Know your Compiler and Architecture

- On target fault-injection → entire fault space
  - Each and every register, flag, instruction and execution path
  - FAIL\* fault injection framework [6]
- → Violation of predicted fault-detection capabilities

#### Architecture specifics

- Absence of compound test-and-branch (e.g., IA32 architecture)
- Control-flow information is stored in single bit
- → Redundancy is lost
- → Additional range checks

#### Undefined Execution Environment

- Zombie values  $\rightarrow$  leaking from caller to voter function
- Compiler laziness leaves encoded values in registers
- → Isolation assumptions violated
- → Cleaning local storage restores isolation

### $\rightarrow$ Tight feedback loop with fault-injection experiments

![](_page_30_Picture_16.jpeg)

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![](_page_31_Picture_15.jpeg)

### **Evaluation – Experimental Setup**

![](_page_32_Figure_1.jpeg)

Categories: Fail Silent, Masked, Hardware Detected, EAN-Code, Control-Flow, Silent Data Corruption

Outcome:401,592 experimentsEffective:67,617 errors

![](_page_33_Figure_1.jpeg)

- Redundant execution campaign (Interface)
  - Total: ~45,000 Errors

![](_page_33_Picture_4.jpeg)

![](_page_34_Figure_1.jpeg)

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  - Total: ~45,000 Errors
    Unprotected: Suffers from 3,622 corruptions!

![](_page_34_Picture_4.jpeg)

![](_page_35_Figure_1.jpeg)

- Redundant execution campaign (Interface)
  - Total: ~45,000 Errors
    Unprotected: Suffers from 3,622 corruptions!
  - TMR: Suffers from 71 corruptions!

![](_page_35_Picture_5.jpeg)

![](_page_36_Figure_1.jpeg)

- Redundant execution campaign (Interface)
  - Total: ~45,000 Errors
    Unprotected: Suffers from 3,622 corruptions!
  - TMR: Suffers from 71 corruptions!
  - CoRed: Remaining corruptions are covered  $\rightarrow$  0 corruptions

![](_page_36_Picture_6.jpeg)

![](_page_37_Figure_1.jpeg)

Voter campaign

paign

![](_page_37_Picture_4.jpeg)

![](_page_38_Figure_1.jpeg)

![](_page_38_Picture_2.jpeg)

![](_page_39_Figure_1.jpeg)

![](_page_39_Picture_2.jpeg)

![](_page_40_Figure_1.jpeg)

![](_page_41_Figure_1.jpeg)

Eliminate single points of failure [1]

![](_page_41_Picture_3.jpeg)

![](_page_42_Figure_1.jpeg)

#### Eliminate single points of failure [1]

- TMR + Encoding: Combined Redundancy approach
- Key feature: CoRed Dependable Voter

![](_page_42_Picture_5.jpeg)

![](_page_43_Figure_1.jpeg)

### Eliminate single points of failure [1]

- TMR + Encoding: Combined Redundancy approach
- Key feature: CoRed Dependable Voter

### Constrain residual error probability [2]

- Parameterisation guidelines: choosing the right A
- Binary aware implementation: complying with coding theory
- Factor 1000 improvement

#### Dependability as a resource efficient option

Only 7.1% overhead (flight control example)

![](_page_43_Picture_11.jpeg)

![](_page_44_Figure_1.jpeg)

### Eliminate single points of failure [1]

- TMR + Encoding: Combined Redundancy approach
- Key feature: CoRed Dependable Voter

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#### Dependability as a resource efficient option

Only 7.1% overhead (flight control example)

### → Bullet-proof software-based fault tolerance is possible

#### http://www4.cs.fau.de/Research/CoRed

![](_page_45_Picture_1.jpeg)

- (1) Ulbrich, Peter; Hoffmann, Martin; Kapitza, Rüdiger; Lohmann, Daniel; Schmid, Reiner; Schröder-Preikschat, Wolfgang: *"Eliminating Single Points of Failure in Software-Based Redundancy"*, Proceedings of the 9th European Dependable Computing Conference (EDCC '12), 2012.
- (2) Hoffmann, Martin; Ulbrich, Peter; Dietrich, Christian; Schirmeier, Horst; Lohmann, Daniel; Schröder-Preikschat, Wolfgang: *"A Practitioner's Guide to Software-based Soft-Error Mitigation Using AN-Codes"*, Proceedings of the 15th IEEE International Symposium on High Assurance Systems Engineering (HASE '14), 2014.

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- (3) P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modelling the effect of technology trends on the soft error rate of combinational logic," in DSN '02: Proceedings of the 2002 International Conference on Dependable Systems and Networks
- (4) Edmund B. Nightingale, John R Douceur, and Vince Orgovan, Cycles, Cells and Platters: An Empirical Analysis of Hardware Failures on a Million Consumer PCs, in Proceedings of EuroSys 2011
- (5) Forin, "Vital coded microprocessor principles and application for various transit systems", 1989
- (6) Schirmeier, Horst ; Hoffmann, Martin ; Kapitza, Rüdiger ; Lohmann, Daniel ; Spinczyk, Olaf : "FAIL: Towards a Versatile Fault-Injection Experiment Framework", 25th International Conference on Architecture of Computing Systems, 2012

![](_page_46_Picture_5.jpeg)